N-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4174 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.
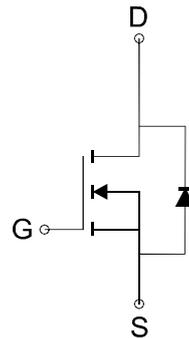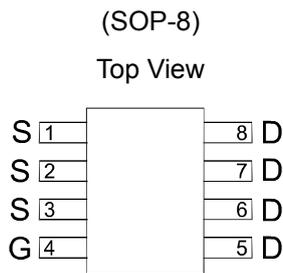
FEATURES

● $R_{DS(ON)} \leqq 6.2m\Omega @ V_{GS}=10V$

● $R_{DS(ON)} \leqq 11m\Omega @ V_{GS}=4.5V$

● Super high density cell design for extremely low $R_{DS(ON)}$

● Exceptional on-resistance and maximum DC current capability

APPLICATIONS

● Power Management in Note book
● Portable Equipment
● Battery Powered System
● DC/DC Converter
● Load Switch
● DSC
● LCD Display inverter

PIN   CONFIGURATION

(SOP-8)

Top View

Ordering Information: ME4174 (Pb-free)

ME4174-G (Green product-Halogen free)

N-Channel MOSFET

Absolute Maximum Ratings ($T_A=25℃$ Unless Otherwise Noted)

Parameter		Symbol	Steady State		Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current($T_j=150℃$)	$T_A=25℃$	I_D	15.8		A
	$T_A=70℃$		12.7		
Pulsed Drain Current		I_{DM}	64		A
Maximum Power Dissipation	$T_A=25℃$	P_D	2.5		W
	$T_A=70℃$		1.6		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	Steady State	50	℃/W

*The device mounted on $1in^2$ FR4 board with 2 oz copper

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N-Channel 30V (D-S) MOSFET

Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

| Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, I_D=250μA	1.0		3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=10V, I_D= 30A		5.2	6.2	mΩ
		V_{GS}=4.5V, I_D= 15A		8.2	11	
V_{SD}	Diode Forward Voltage	I_S=20A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Q_g	Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=25A		37		nC
Q_{gt}	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=25A		19		
Q_{gs}	Gate-Source Charge			8		
Q_{gd}	Gate-Drain Charge			9		
C_{iss}	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		1640		pF
C_{oss}	Output Capacitance			260		
C_{rss}	Reverse Transfer Capacitance			84		
R_g	Gate Resistance	f =1MHz		0.9		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V R_G=3Ω		19		ns
t_r	Turn-On Rise Time			15		
$t_{d(off)}$	Turn-Off Delay Time			54		
t_f	Turn-On Fall Time			6.5		

Notes: a. Pulse test: pulse width$\leq$ 300us, duty cycle$\leq$ 2%, Guaranteed by design, not subject to production testing.

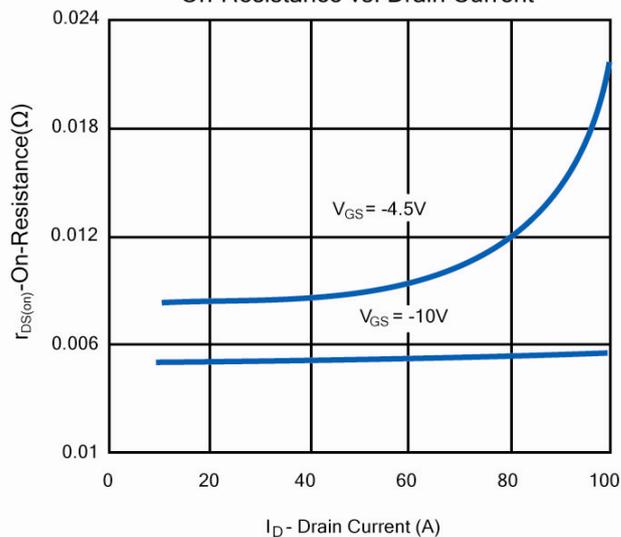b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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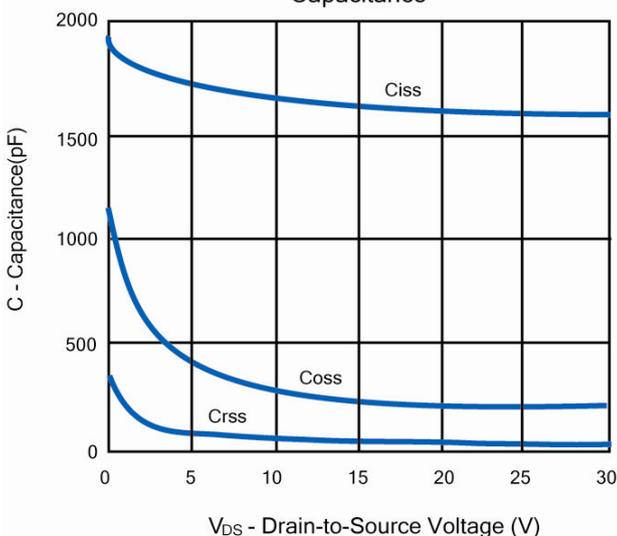## Typical Characteristics (TJ =25℃ Noted)

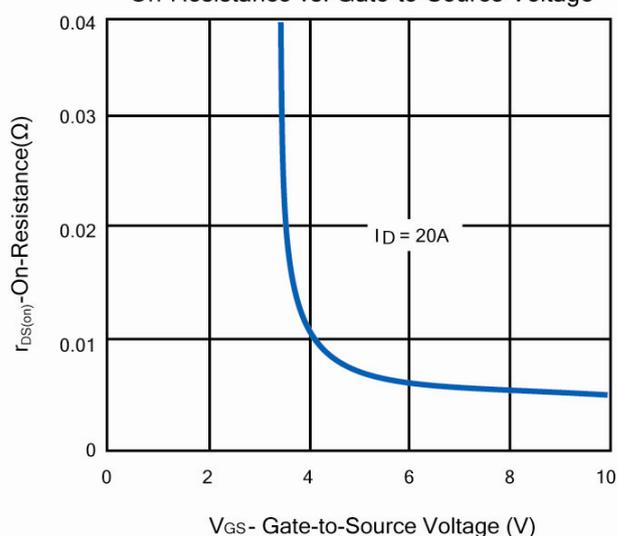### On Resistance vs. Junction Temperature
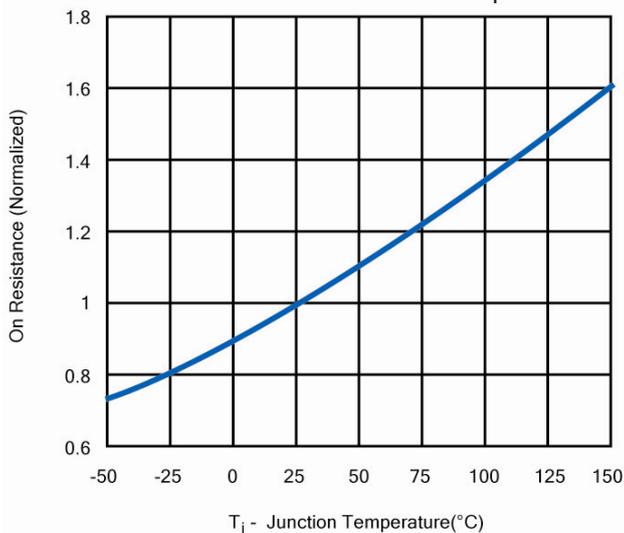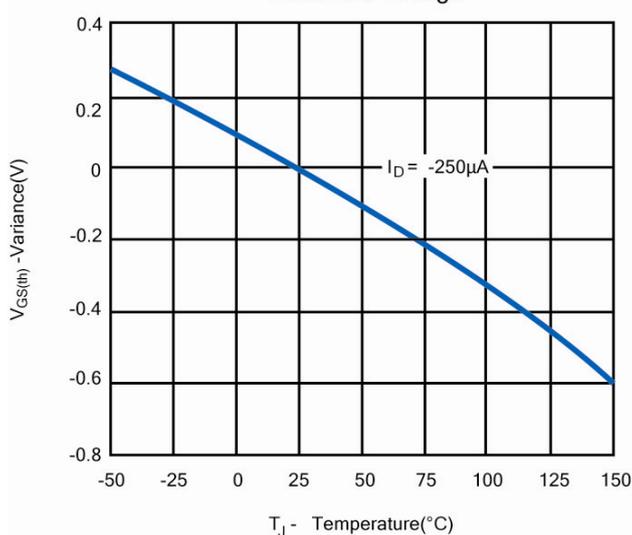

On-Resistance vs. Drain Current
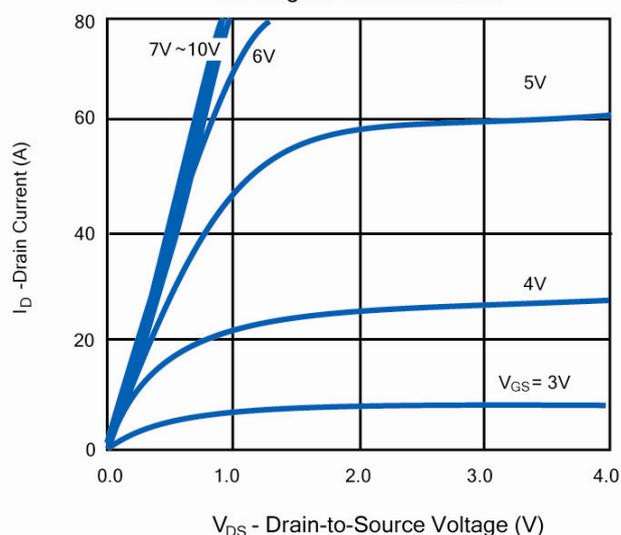

Capacitance

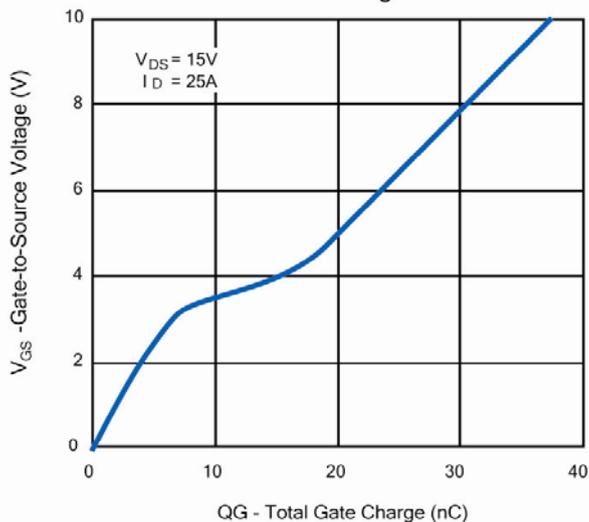### On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

On-Region Characteristics

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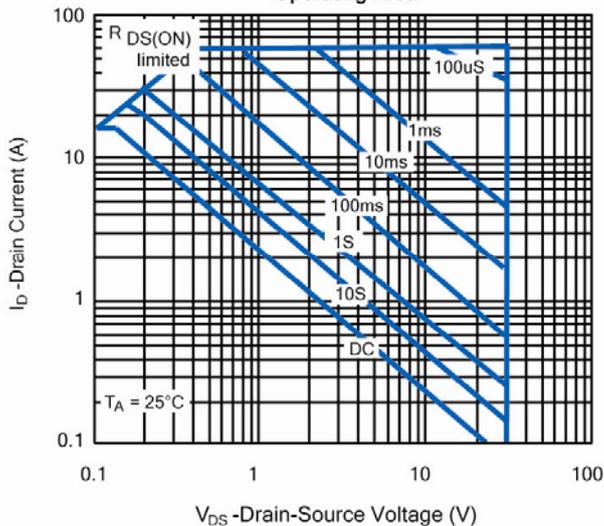
Typical Characteristics (TJ =25℃ Noted)

Gate Charge

$V_{DS} = 15V$
$I_D = 25A$

V_{GS} -Gate-to-Source Voltage (V) vs QG - Total Gate Charge (nC)

Source to Drain Diode Forward Voltage

I_S-Source Current (A) vs V_{SD} -Source-to-Drain Voltage (V)

$T_A = 25°C$
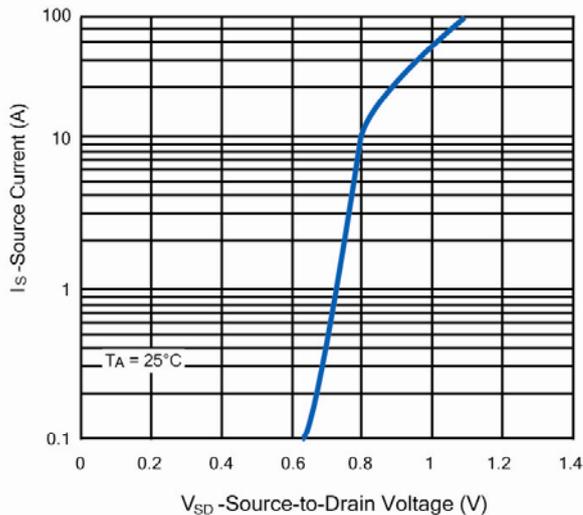
Maximum Forward Biased Safe Operating Area

$R_{DS(ON)}$ limited

100uS
1ms
10ms
100ms
1S
10S
DC

$T_A = 25°C$

I_D -Drain Current (A) vs V_{DS} -Drain-Source Voltage (V)

Single Pulse Maximum Power Dissipation

$T_A = 25°C$

$P(pk)$,-Peak Transient Power (W) vs t_1 - Time (sec)
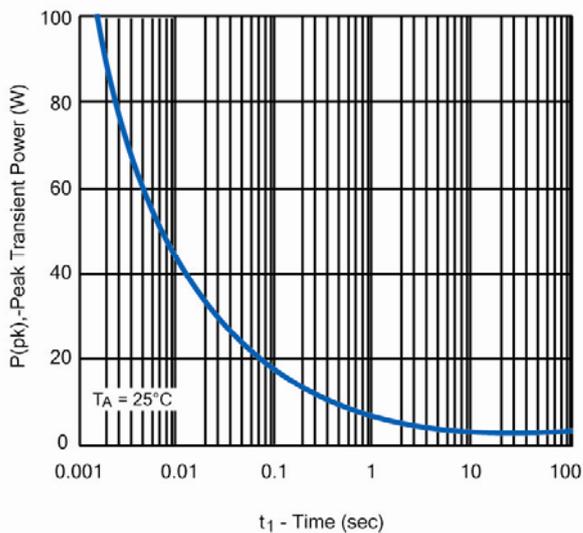
Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Effective Transient Thermal Impedance

70%
50%
30%
10%
5%
2%
1%
0.5%
0.2%

Single Pulse Curve

Square Wave Pulse Duration (sec)

Notes:

P_{DM}

t_1 t_2

1. Duty Cyde, $D = \dfrac{t_1}{t_2}$
2. Per Unit Base = R_{thJA} = 54°C/W
3. $T_{JM} - T_A = P_{DM} Z_{thJA}{}^{(t)}$
4. Surface Mounted