

# MSL60P03

## P-Channel 60-V (D-S) MOSFET

### Description

The MSL60P03 is the highest performance P-ch MOSFETs with super high dense cell design for low  $R_{DS(ON)}$  and gate charge for high efficiency fast switching applications.

The device meets the RoHS and Green Product requirement with full function reliability approved.

### Features

- Low Reverse Transfer Capacitance
- High Switching Speed
- Improved dv/dt Capability
- Low Gate Charge
- Green Device Available

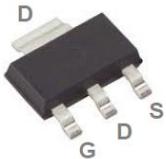
### Typical Applications

- Motor Control
- Net Working
- LED Applications

Package type : SOT-223

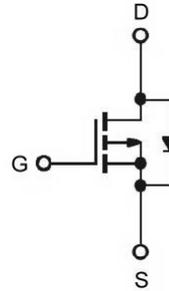
### Packing & Order Information

2,500/Reel

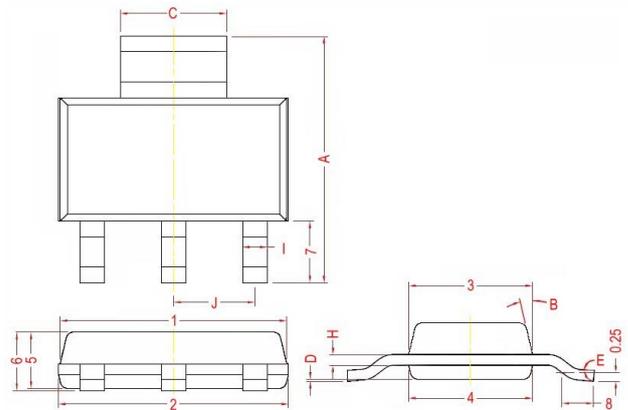


RoHS Compliant

### Graphic Symbol

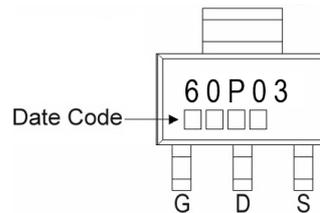


### Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.70	7.30	1	6.30	6.80
C	2.90	3.10	2	6.30	6.80
D	0.02	0.10	3	3.30	3.70
E	0°	10°	4	3.30	3.70
I	0.60	0.80	5	1.40	1.80
H	0.25	0.35	6	1.50	1.80
B	13° Typ.		7	1.55	1.95
J	2.30 Ref.		8	0.80	1.10

### Marking



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#### MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

##### Absolute Maximum Ratings (unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-Source Voltage	-60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>1</sup> ( $T_A = 25^\circ\text{C}$ )	-3.2	A
	Continuous Drain Current <sup>1</sup> ( $T_A = 70^\circ\text{C}$ )	-2.5	A
$I_{DM}$	Pulsed Drain Current <sup>1,2</sup> ( $T_A = 25^\circ\text{C}$ )	-12	A
$P_D$	Power Dissipation <sup>3</sup> ( $T_A = 25^\circ\text{C}$ )	2	W
$T_J/T_{STG}$	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$

##### Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient <sup>1</sup>	62.5	$^\circ\text{C/W}$

##### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1.0	-	-2.5	V
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-60	-	-	V
$I_{GSS}$	Gate-Source Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = -48\text{V}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -48\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$	-	-	-5	
$R_{DS(on)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS} = -10\text{V}, I_D = -2\text{A}$	-	110	130	m $\Omega$
		$V_{GS} = -4.5\text{V}, I_D = -1.5\text{A}$	-	140	190	
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$I_S = -1.0\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	-	-	-1.2	V
$I_S$	Continuous Source Current <sup>1,4</sup> (Diode)	$V_G = V_D = 0\text{V}$ , Force Current	-	-	-3.2	A

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#### Dynamic and switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	V <sub>DS</sub> = -20V	--	5.9	--	nC
Q <sub>gs</sub>	Gate-Source Charge	I <sub>D</sub> = -2A	--	2.9	--	
Q <sub>gd</sub>	Gate-Drain Charge	V <sub>GS</sub> = -4.5V	--	1.8	--	
t <sub>d(on)</sub>	Turn-On Delay Time <sup>2</sup>	V <sub>DD</sub> = -12V	--	10	--	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> = -1A	--	17	--	
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = -10V	--	22	--	
t <sub>f</sub>	Fall Time	R <sub>G</sub> = 3.3Ω	--	21	--	
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> = -15V	--	715	--	pF
C <sub>OSS</sub>	Output Capacitance	V <sub>GS</sub> = 0V	--	51	--	
C <sub>RSS</sub>	Reverse Transfer Capacitance	f = 1.0MHz	--	34	--	

#### Notes

1. Surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The power dissipation is limited by 150°C junction temperature.
4. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

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### P-Channel 60-V (D-S) MOSFET

- Typical Electrical Characteristics

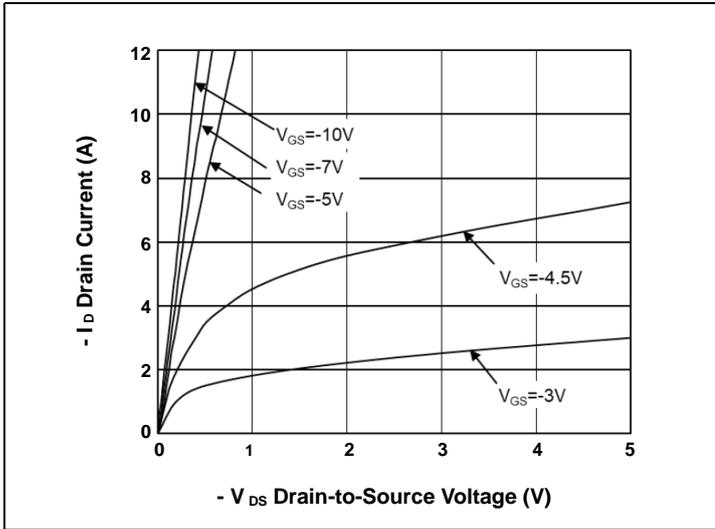


FIG.1-Typical Output Characteristics

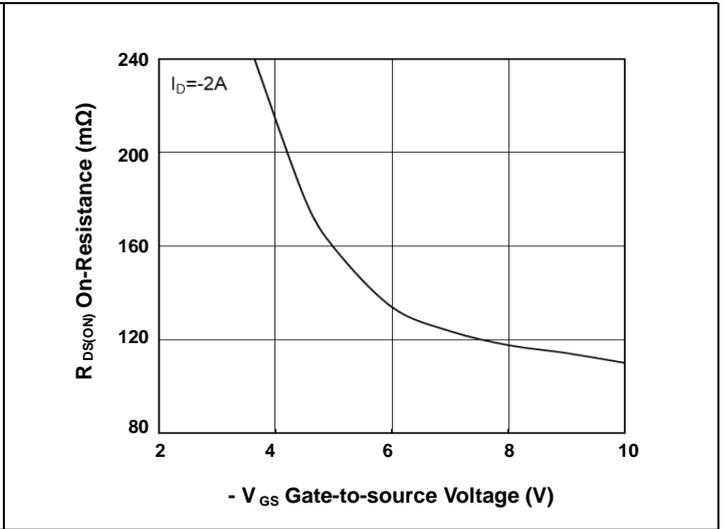


FIG.2-On-Resistance vs. G-S Voltage

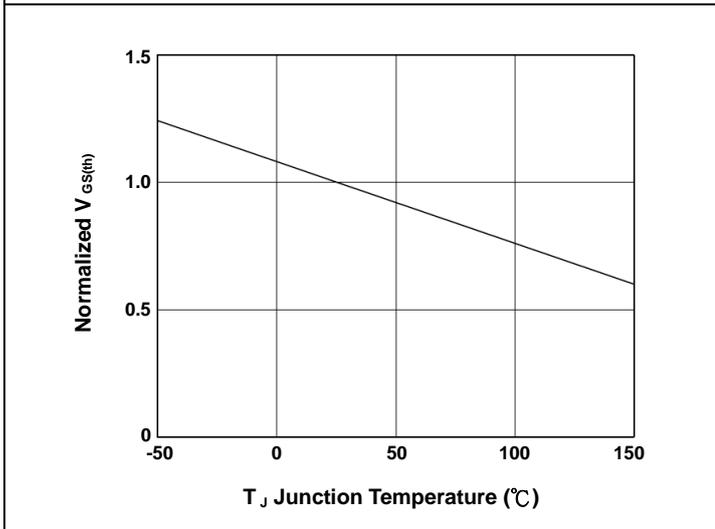


FIG.3-Normalized  $V_{GS(th)}$  vs.  $T_J$

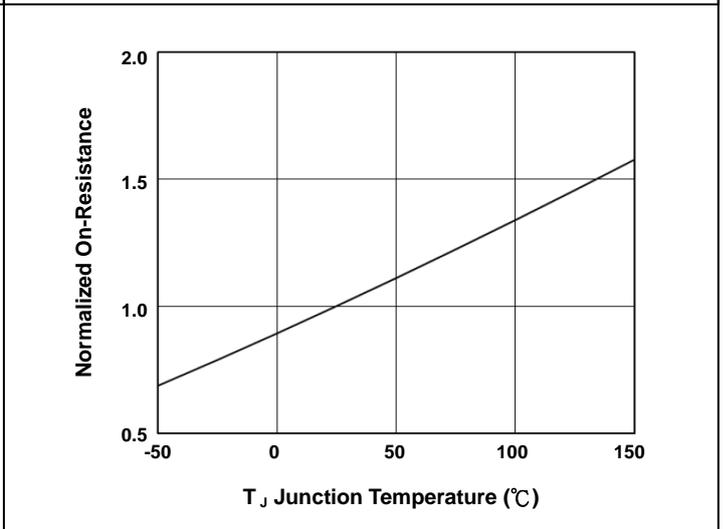


FIG.4-Normalized  $R_{DS(on)}$  vs.  $T_J$

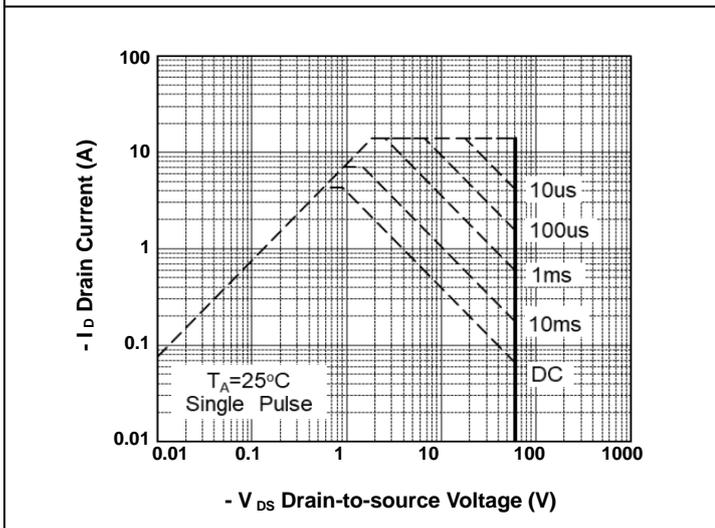


FIG.5-Safe Operating Area

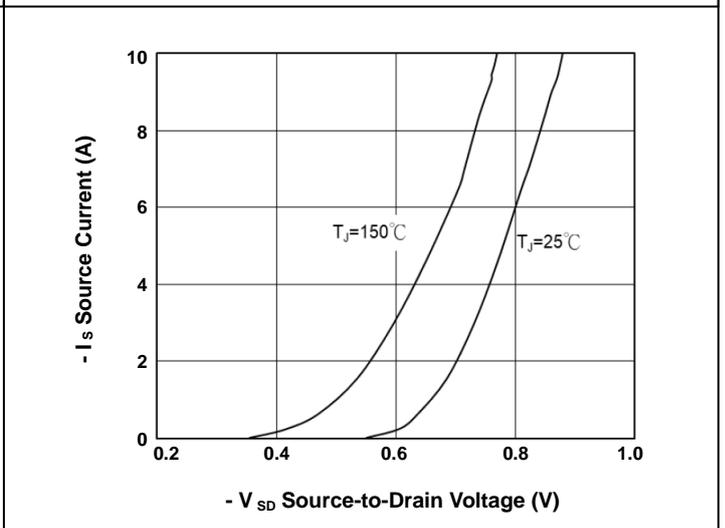


FIG.6-Source Drain Forward Characteristics

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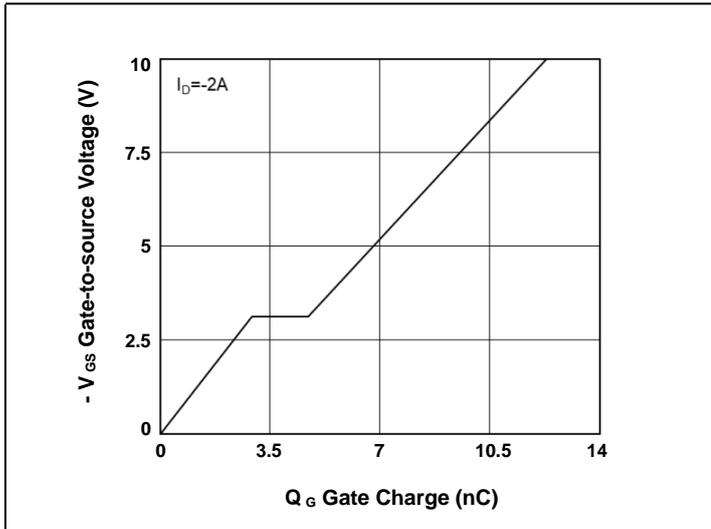


FIG.7-Gate Charge Characteristics

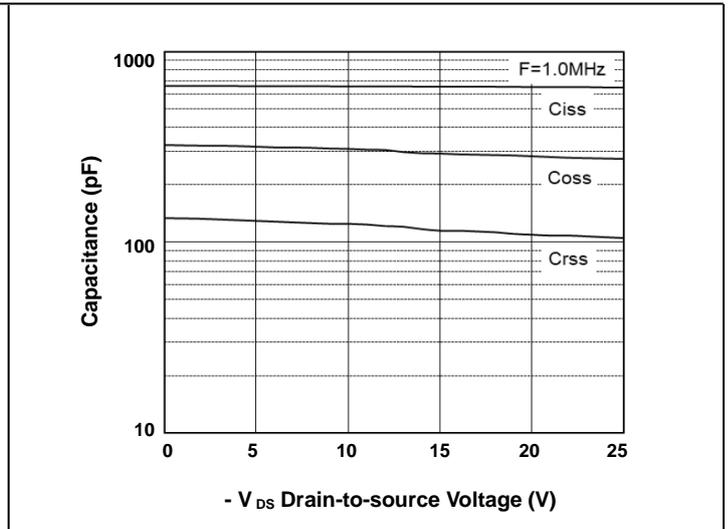


FIG.8-Capacitance Characteristics

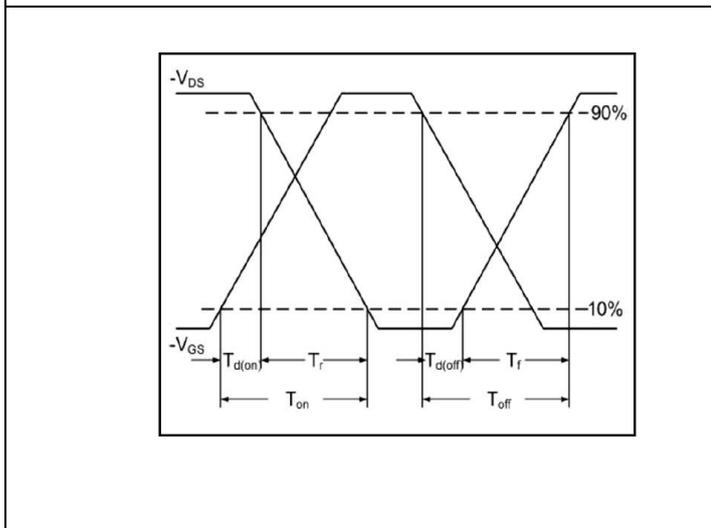


FIG.9-Switching Time Waveform

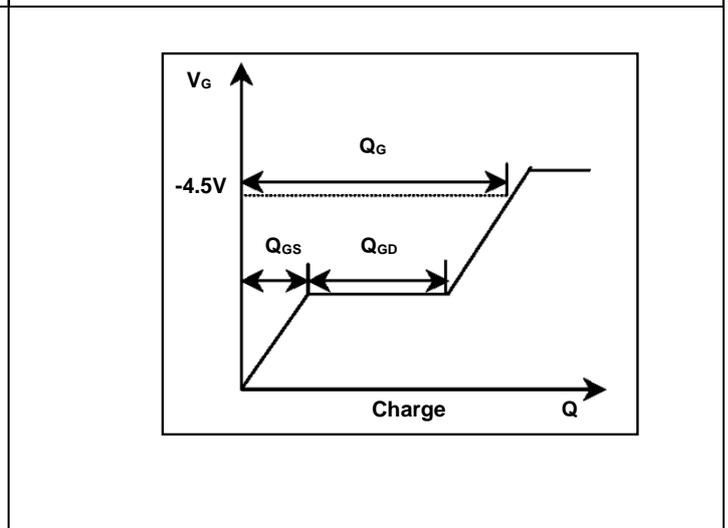


FIG.10-Gate Charge Waveform

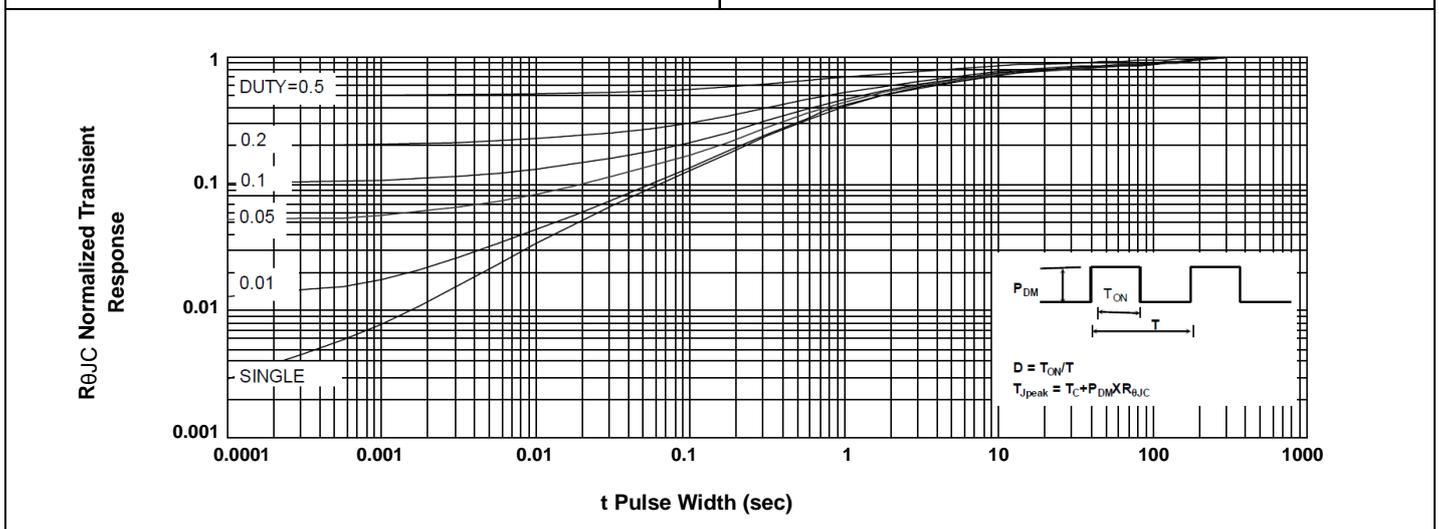


FIG.11-Normalized Maximum Transient Thermal Impedance

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