

SuperMOS - TO-252 -40V BV_{DSS} , 13m Ω $R_{DS(on)}$, P-channel MOSFET

1. Description

The ESE40P40K is P-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. Device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product ESE40P40K is Pb-free.

2. Features

- -40V, $R_{DS(ON)}=13m\Omega(TYP.) @V_{GS}=-10V$
- $R_{DS(ON)}=17m\Omega(TYP.) @V_{GS}=-4.5V$
- Fast Switching
- High density cell design for low $R_{DS(on)}$
- Material: Halogen free
- Reliable and rugged
- Avalanche Rated
- Low leakage current

3. Applications

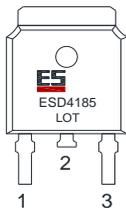
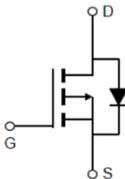
- PWM applications
- Load switch
- Power management in portable/desktop PCs
- DC/DC conversion

100% UIS TESTED!

4. Ordering Information

Part Number	Package	Marking	Material	Packing	Quantity per reel	Flammability Rating	Reel size
ESE40P40K	TO-252	ESD4185/lot	Halogen free	Tape & Reel	2,500 PCS	UL 94V-0	13 inches

5. Pin Configuration and Functions

Pin	Function	Outline	Circuit Diagram
1	Gate	Note c 	
3	Source		
2	Drain		

6. Specification

Absolute Maximum Rating & Thermal Characteristics

Ratings at 25 °C ambient temperature unless otherwise specified.

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	BV_{DSS}	-40	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	-45
		$T_C=75^\circ\text{C}$	-34
Maximum Power Dissipation	P_D	$T_C=25^\circ\text{C}$	52
		$T_C=75^\circ\text{C}$	32
Pulsed Drain Current ^a	I_{DM}	-180	A
Avalanche Current, Single Pulsed ^b	I_{AS}	-33	A
Avalanche Energy, Single Pulsed ^b	E_{AS}	163	mJ
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typ	Max	Unit
Junction-to-Ambient Thermal Resistance	$t \leq 10 \text{ s}$	$R_{\theta JA}$	15	20	°C/W
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	2	2.4	

Note:

- a: Repetitive rating, pulse width limited by junction temperature, $t_p=10\mu\text{s}$, Duty Cycle=1%
- b: EAS condition: $T_J=25^\circ\text{C}$, $V_{DD}=-30\text{V}$, $V_G=-10\text{V}$, $L=0.3\text{mH}$, $R_g=25\Omega$
- c: This diagram is only an electrical schematic, and the actual pin size is based on POD.

Electrical Characteristics

At TA = 25°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-40V$			-1	μA
Gate-to-source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-1.6	-2.0	V
Drain-to-source On-resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-20A$		13	16	m Ω
		$V_{GS}=-4.5V, I_D=-15A$		17	20	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	$V_{GS}=0V, V_{DS}=-15V,$ $f=1MHz$		2500		pF
Output Capacitance	C_{OSS}			260		
Reverse Transfer Capacitance	C_{RSS}			180		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS}=-10V, V_{DS}=-15V,$ $I_D=-20A$		42		nC
Gate-to-Source Charge	Q_{GS}			7		
Gate-to-Drain Charge	Q_{GD}			8.8		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS}=-10V, V_{DS}=-15V,$ $R_L=1\Omega, R_G=3\Omega$		10		ns
Rise Time	t_r			20		
Turn-Off Delay Time	$t_{d(OFF)}$			55		
Fall Time	t_f			30		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	$V_{GS}=0V, I_{SD}=-1A$		-0.7	-1.5	V

7. Typical Characteristic

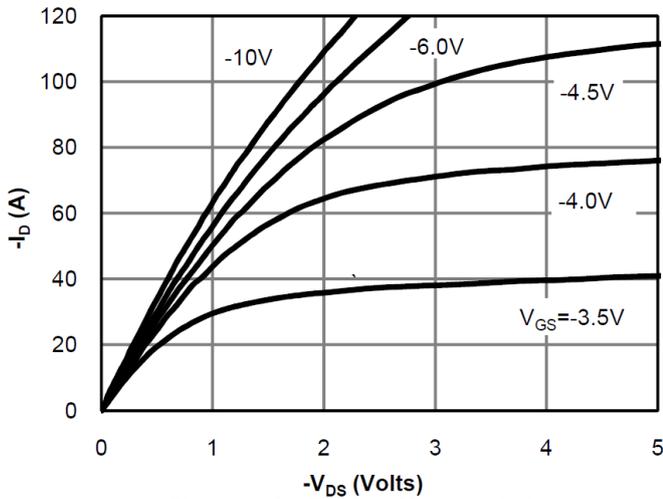


Figure 1: On-Region Characteristics

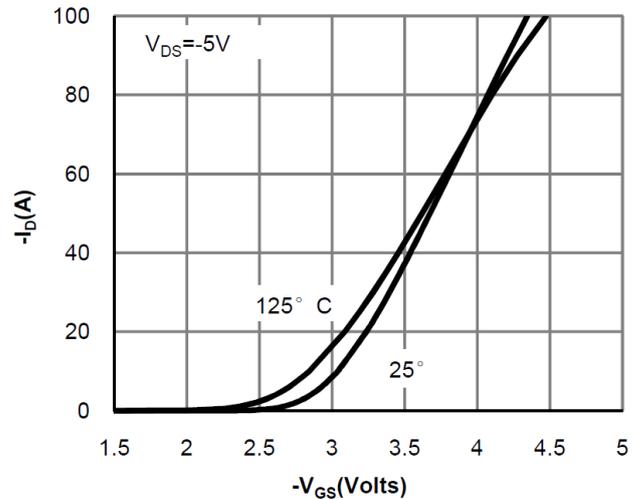


Figure 2: Transfer Characteristics

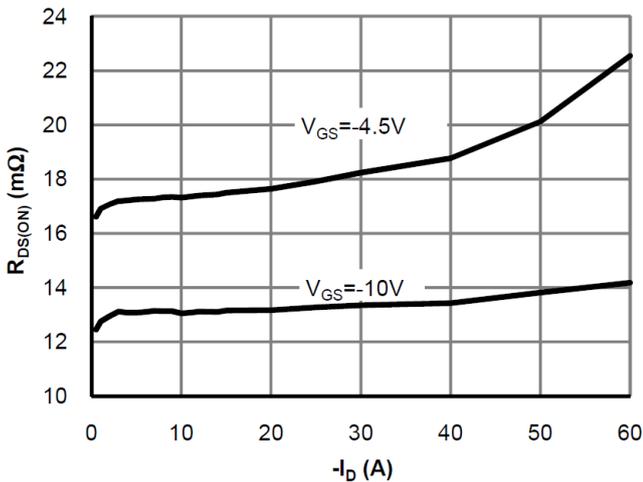


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

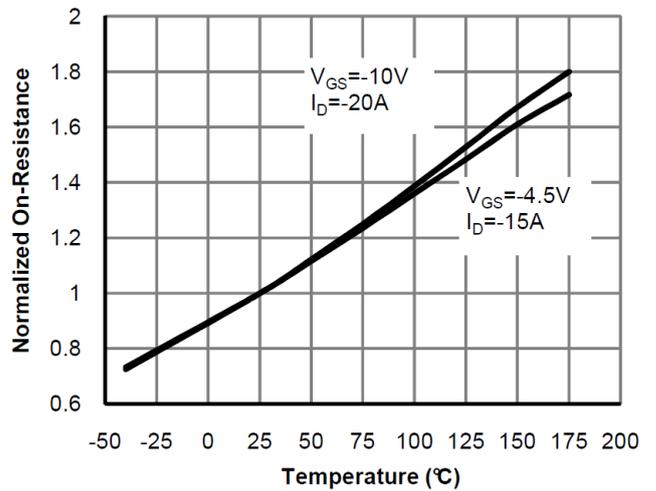


Figure 4: On-Resistance vs. Junction Temperature

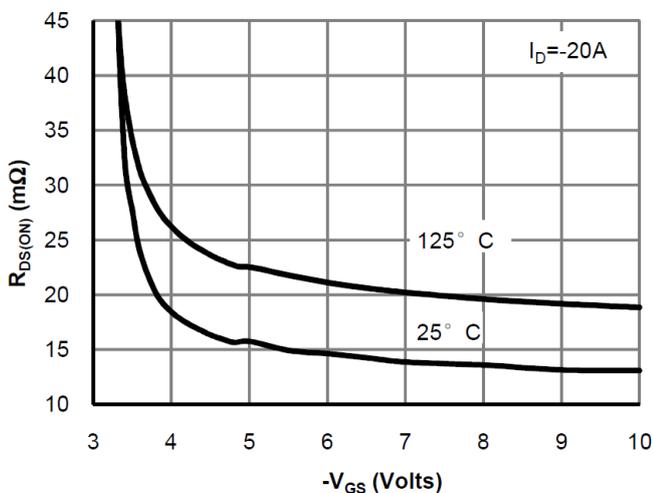


Figure 5: On-Resistance vs. Gate-Source Voltage

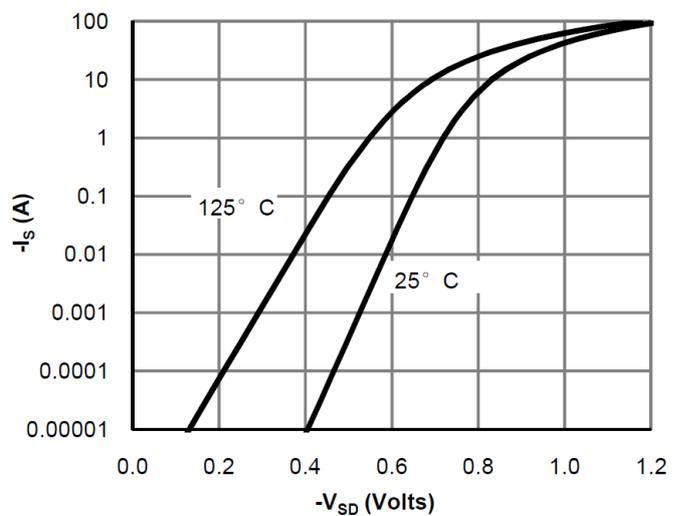


Figure 6: Body-Diode Characteristics

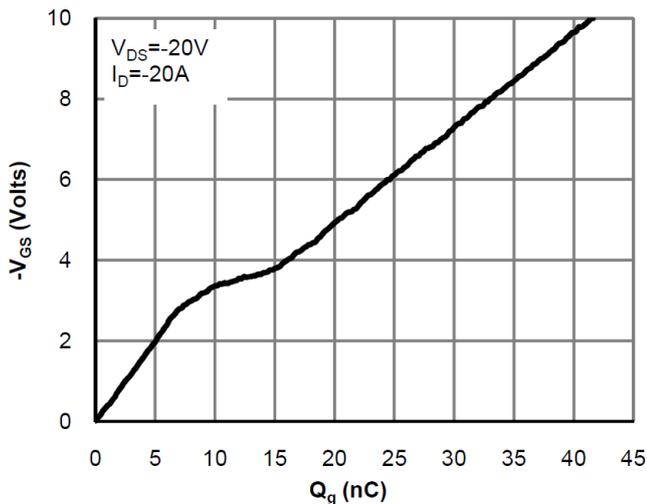


Figure 7: Gate-Charge Characteristics

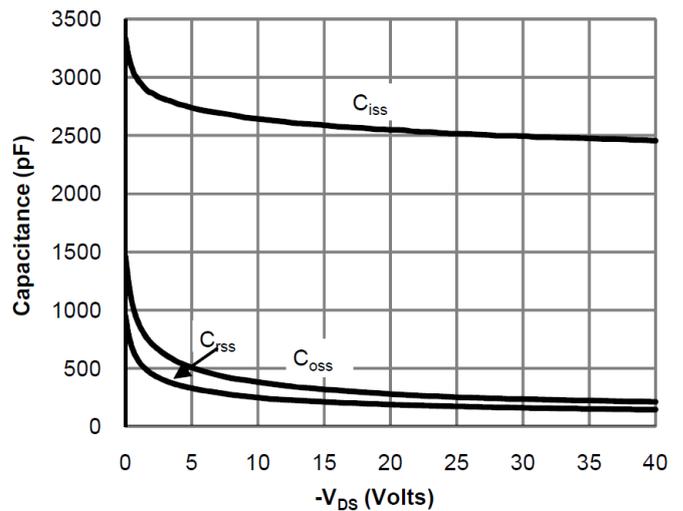


Figure 8: Capacitance Characteristics

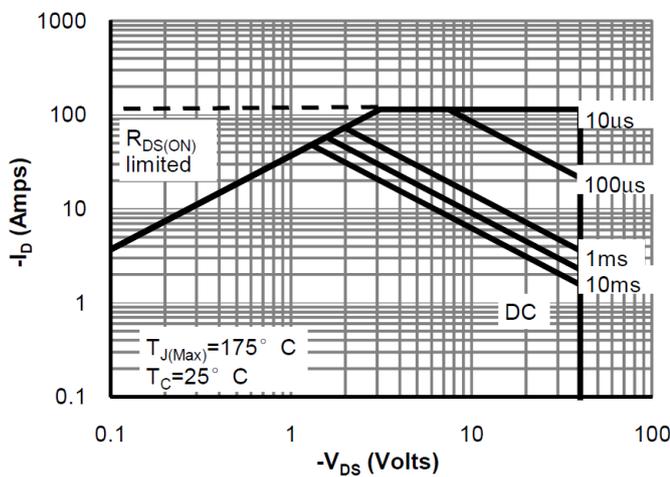


Figure 9: Maximum Forward Biased Safe Operating Area

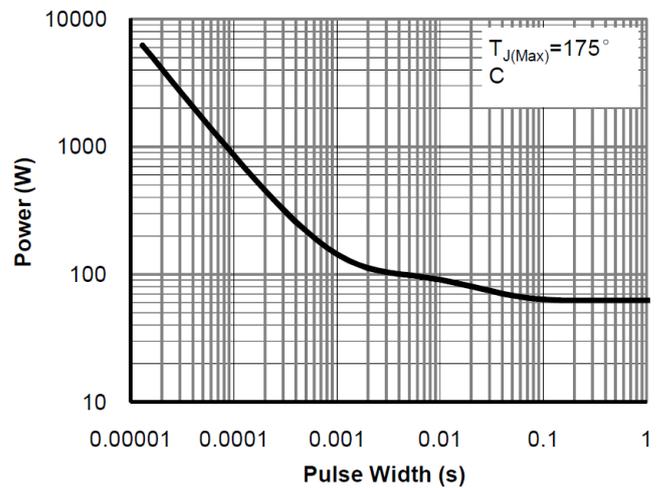


Figure 10: Single Pulse Power Rating Junction-to-Case

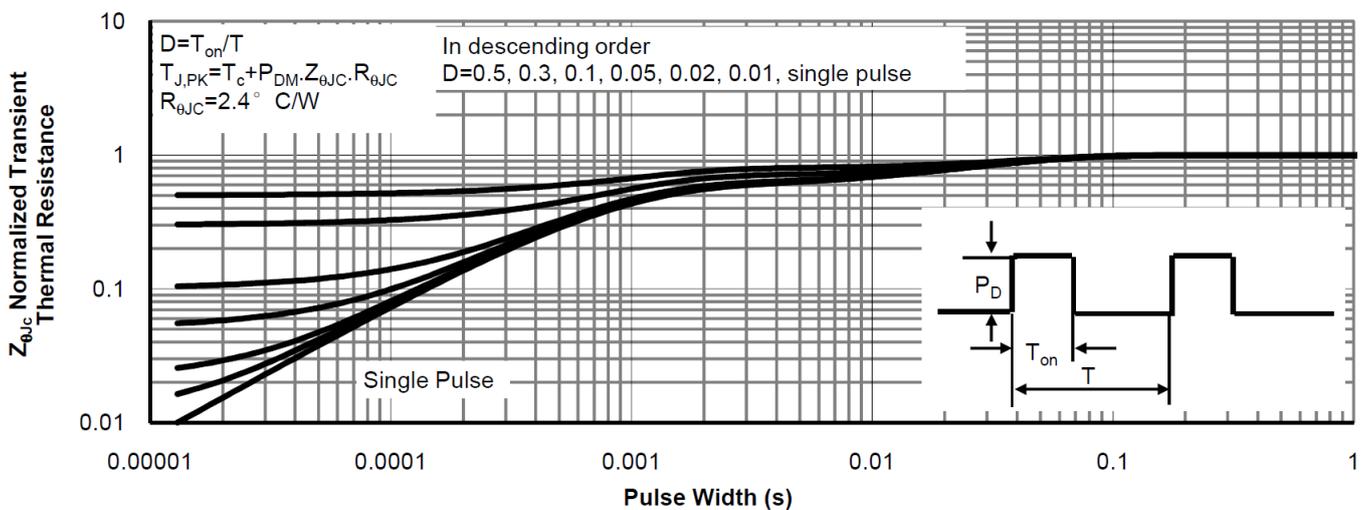
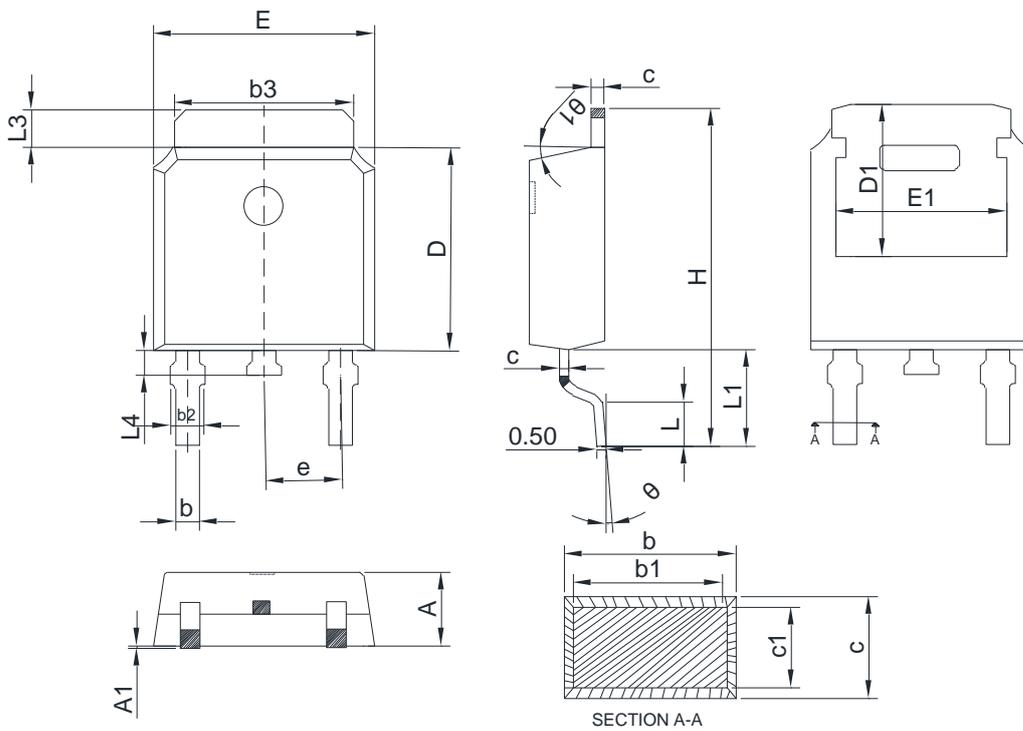


Figure 11: Normalized Maximum Transient Thermal Impedance

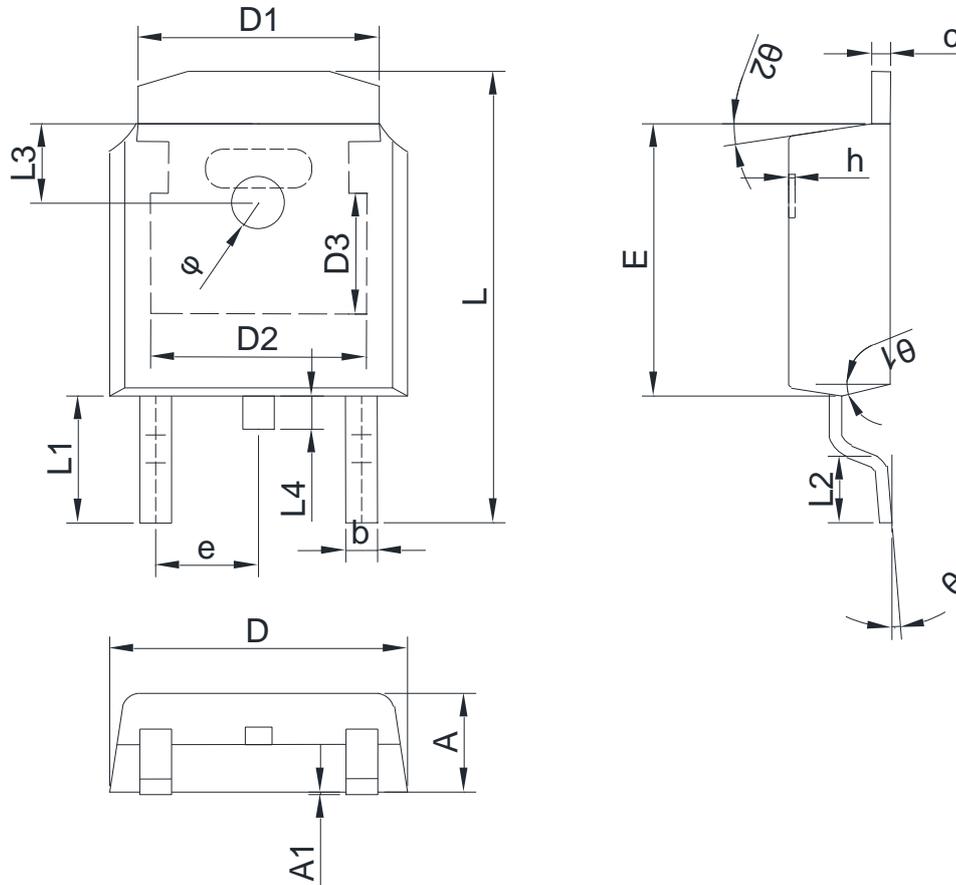
8. Dimension (TO-252)

POD A



COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER							
SYMBOL	MIN	TYP	MAX	SYMBOL	MIN	TYP	MAX
A	2.20	2.30	2.40	D1	5.21	-	-
A1	0.00	-	0.12	E	6.50	6.60	6.70
b	0.65	-	0.89	E1	4.32	-	-
b1	0.64	0.76	0.79	H	9.70	9.95	10.20
b2	0.76	0.86	1.10	L	1.40	1.50	1.60
b3	5.20	5.33	5.46	L1	2.84REF		
c	0.48	-	0.60	e	2.29BSC		
c1	0.47	0.51	0.55	θ	0°	-	10°
D	6.00	6.10	6.20	θ1	0°	-	15°
L3	0.90	-	1.27	L4	0.60	0.80	1.00

POD B



COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER							
SYMBOL	MIN	TYP	MAX	SYMBOL	MIN	TYP	MAX
A	2.200	2.300	2.400	h	0.000	0.100	0.200
A1	0.000		0.127	L	9.900	10.100	10.300
b	0.640	0.690	0.740	L1	2.888 REF		
c(电镀后)	0.460	0.520	0.580	L2	1.400	1.550	1.700
D	6.500	6.600	6.700	L3	1.600 REF		
D1	5.334 REF			L4	0.600	0.800	1.000
D2	4.826 REF			phi	1.100	1.200	1.300
D3	3.166 REF			theta	0°		8°
E	6.000	6.100	6.200	theta1	9° TYP		
e	2.286 TYP			theta2	9° TYP		

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