SP30N03NJ

30V N-Channel MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
30V	3.2mΩ@10V	65A
	4.5mΩ@4.5V	

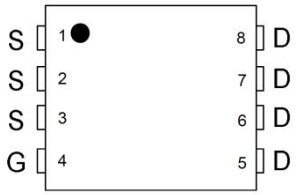
Feature

- VDS =30V,ID=65A
- RDS(ON) typ 3.2mΩ @ VGS=10V
- High density cell design for ultra low Rdson
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation

Application

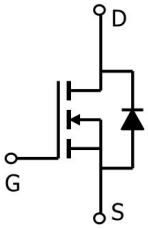
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Package

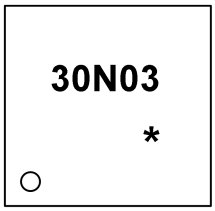


PDFN3X3-8L

Circuit diagram



Marking



30N03 =Device Code
*** =Month Code**

Absolute maximum ratings (Ta=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous (T_C=25℃)	I_D	65	A
Pulsed Drain Current	I_{DM}	260	A
Maximum Power Dissipation (T_C=25℃)	P_D	36	W
Single pulse avalanche energy (Note 5)	E_{AS}	151	mJ
Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	3.4	℃/W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Electrical characteristics (T_A=25 °C, unless otherwise noted)

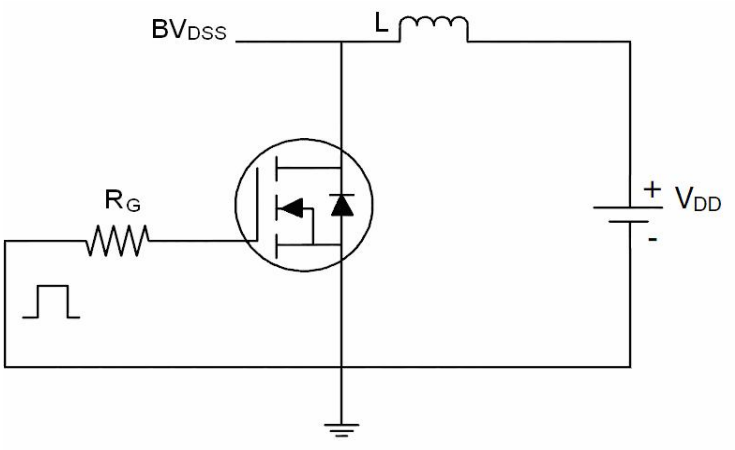
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	30		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1	1.5	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	3.2	4.2	mΩ
		V_{GS}=4.5V, I_D=15A	-	4.5	6	
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V, F=1.0MHz	-	3600	-	PF
Output Capacitance	C_{oss}		-	380	-	PF
Reverse Transfer Capacitance	C_{rss}		-	290	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=15V,I_D=20A V_{GS}=10V,R_{GEN}=3Ω	-	12	-	nS
Turn-on Rise Time	t_r		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	40	-	nS
Turn-Off Fall Time	t_f		-	14	-	nS
Total Gate Charge	Q_g	V_{DS}=15V,I_D=45A, V_{GS}=10V	-	60	-	nC
Gate-Source Charge	Q_{gs}		-	8.2	-	nC
Gate-Drain Charge	Q_{gd}		-	16.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	45	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 20A di/dt = 100A/μs(Note3)	-	29	-	nS
Reverse Recovery Charge	Qrr		-	32	-	nC

Notes:

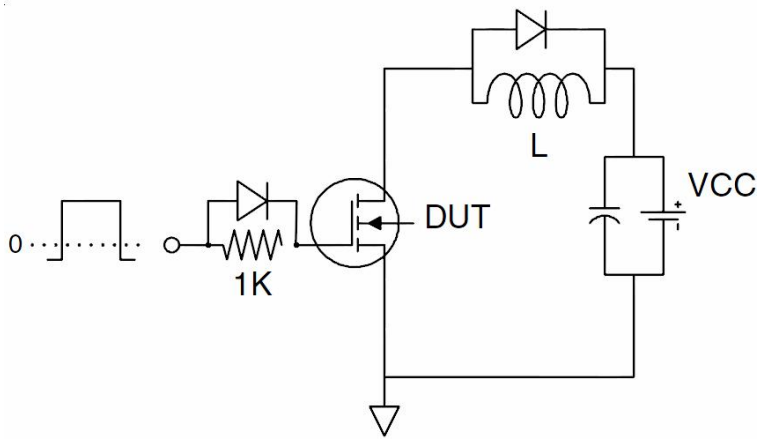
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃, VDD=15V,VG=10V,L=0.1mH, Rg=25Ω,;

Test Circuit

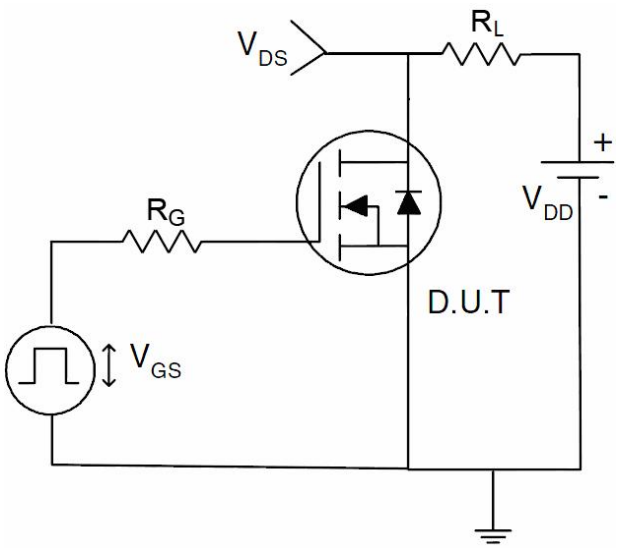
1) EAS Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Characteristics

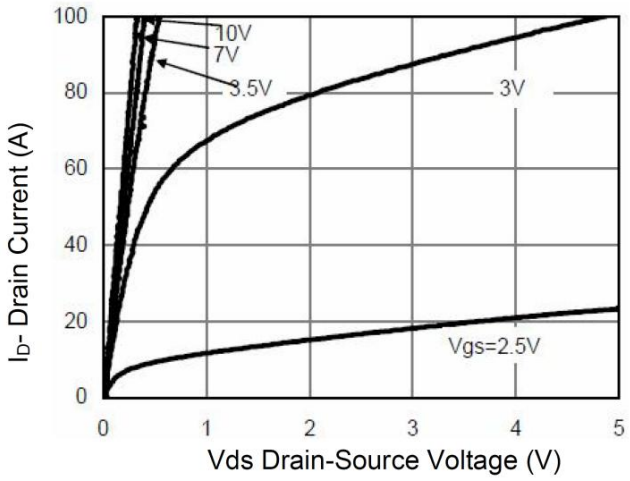


Figure 1 Output Characteristics

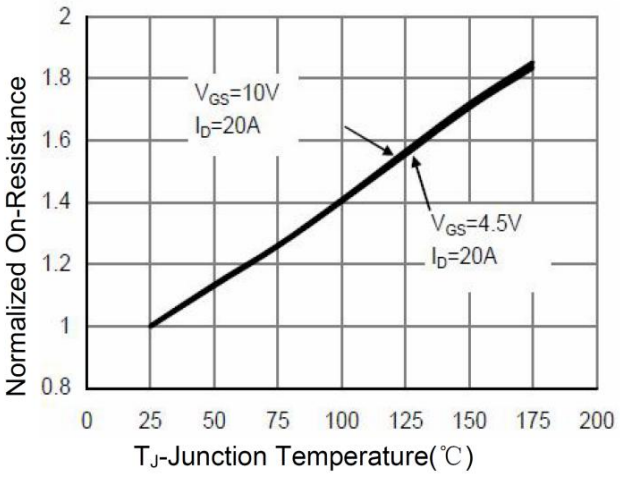


Figure 4 Rdson-Junction Temperature

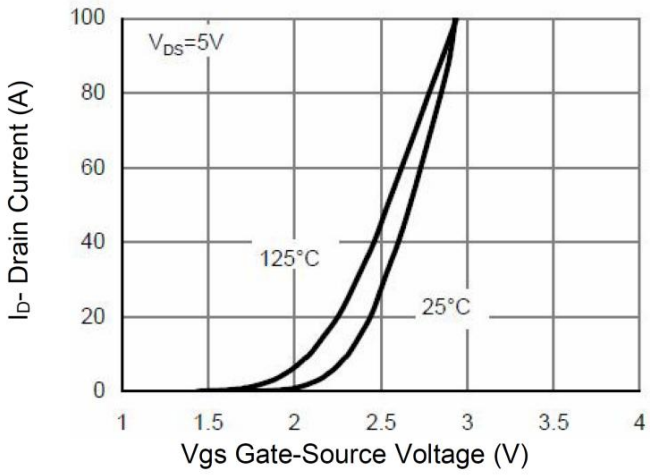


Figure 2 Transfer Characteristics

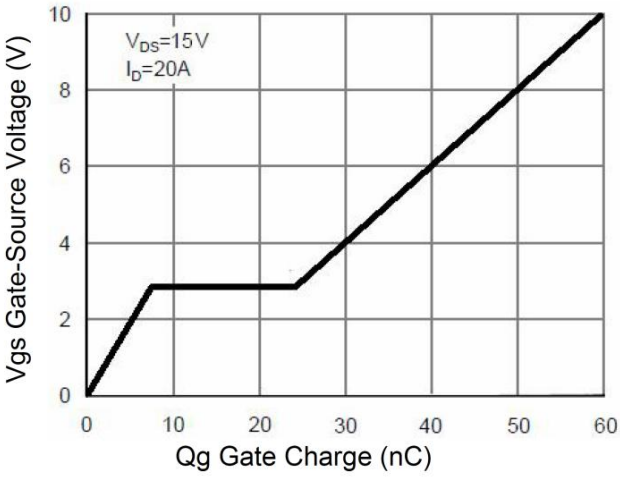


Figure 5 Gate Charge

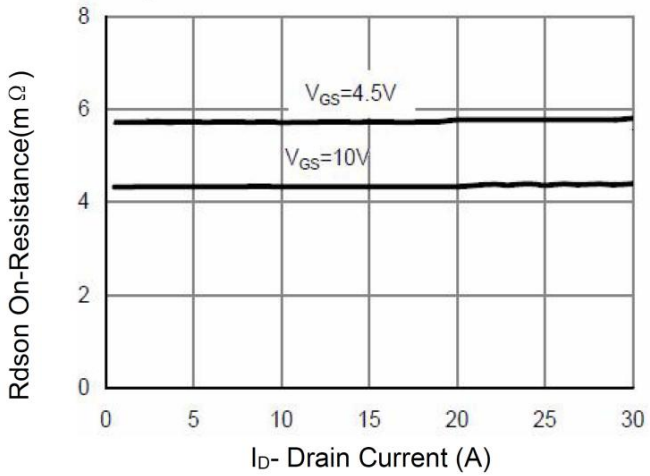


Figure 3 Rdson- Drain Current

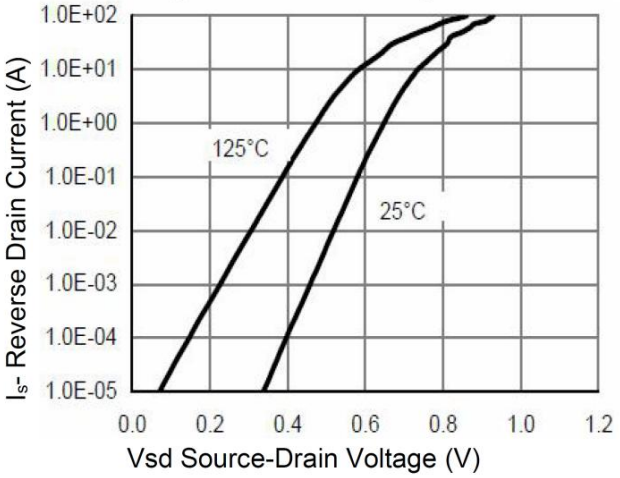


Figure 6 Source- Drain Diode Forward

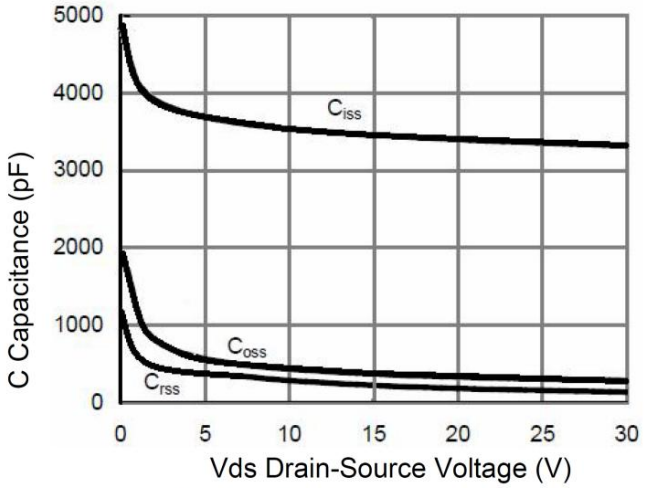


Figure 7 Capacitance vs Vds

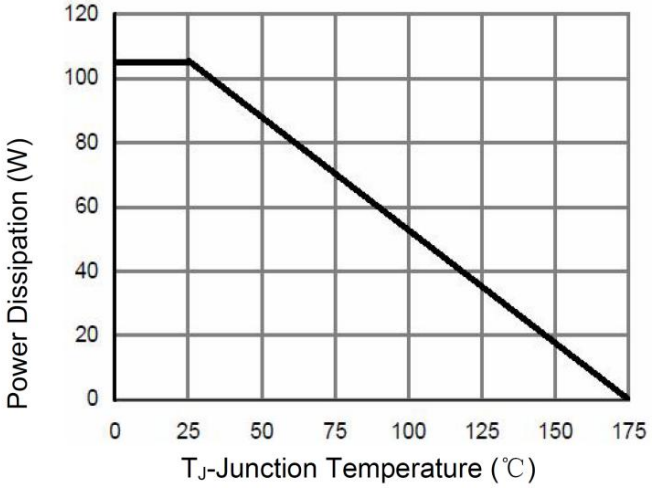


Figure 9 Power De-rating

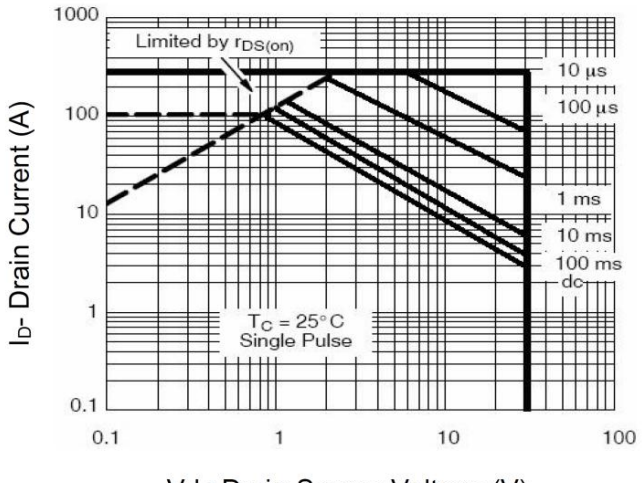


Figure 8 Safe Operation Area

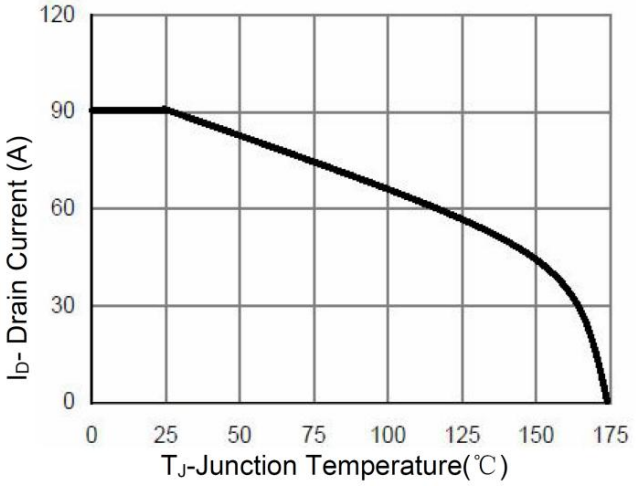


Figure 10 ID Current Derating

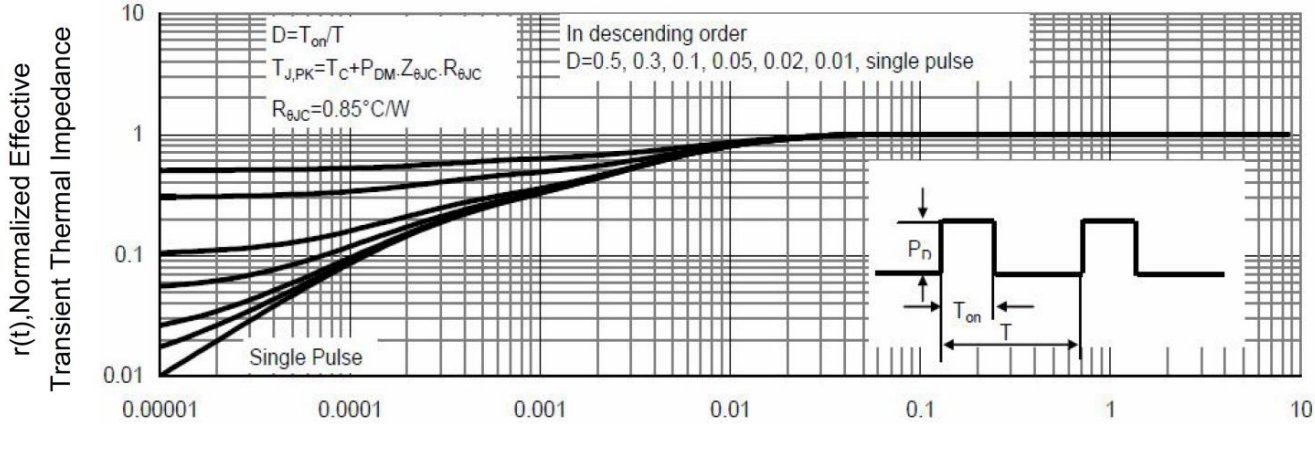
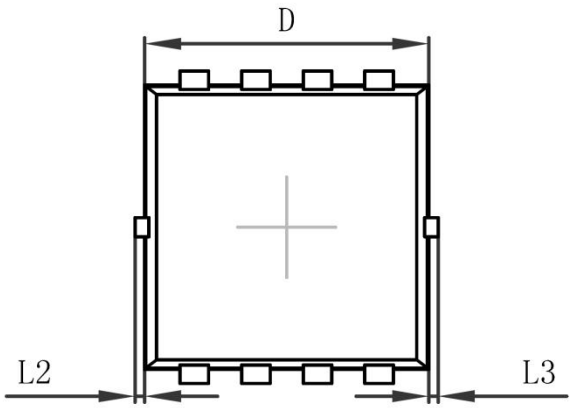
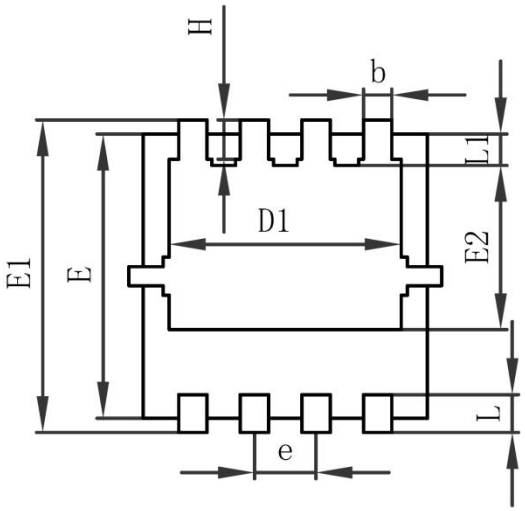


Figure 11 Normalized Maximum Transient Thermal Impedance

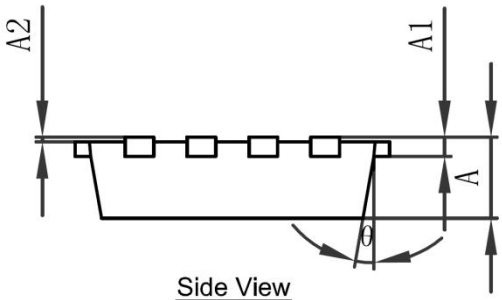
PDFN3X3-8L Package Information



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

制 修 订 记 录					
文件版本	制修日期	修订页次	修订人	变更内容	
1.0	2019/12/31		张功杰	建立规格书	
1.1	2021/10/26		王余林	更换晶圆版本	
1.2	2021/12/27		王余林	放宽RDSON上限	
1.3	2022/1/11		王余林	更新10V下RDSON(typ)&放宽RDSON上限	
1.4	2022/12/12		覃源	根据JJW wafer更新ID/Rdson数据	
批准		审核		编制	
日期		日期		日期	