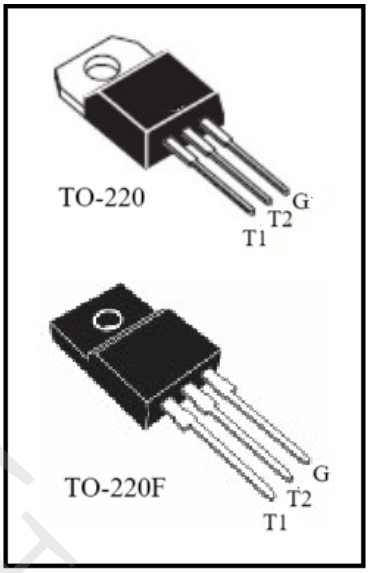
鼎德丰
DING DE FENG

TRIAC BTA16

FEATURES

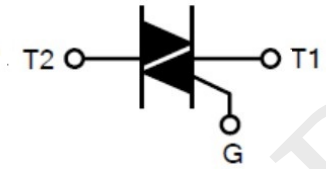
- Glass Passivated Junctions
- High voltage and surge capability
- Low Thermal Resistance and Durability
- Low thermal resistance insulation ceramic
- Insulating Voltage2500V(RMS)



APPLICATIONS

- Mains power AC switching
- Static relays
- Light dimmers
- Heater Control
- Motor Speed Controller

SYMBOL:



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL		VALUE		UNIT
Repetitive Peak Off-State Voltages	$V_{DRM,}$ V_{RRM}	4Q	BTA16-600(C/B)	600	V
			BTA16-800(C/B)	800	
		3Q	BTA16-600(SW/CW/BW)	600	
			BTA16-800(SW/CW/BW)	800	
RMS on-State Current	$I_{T(RMS)}$		16		A
Non-Repetitive Peak On-State Current	I_{TSM}		160		A
I^2t for fusing	I^2t		144		A^2s
Repetitive rate of rise of on-state current after triggering	di/dt		50		A/uS
Peak gate current	I_{GM}		4		A
Peak Gate Power	P_{GM}		5		W
Average Gate Power	$P_{G(AV)}$		1		W
Operating junction temperature	T_J		-40~+125		℃
Storage Temperature	T_{STG}		-40 ~ +150		℃

ELECTRICAL CHARACTERISTICS (TJ=25°C) (4Q) Standard

Parameter	Symbol	Test Conditions			C	B	Units
Peak Repetitive Forward or Reverse Blocking Current	I_{DRM} I_{RRM}	V_{AK} = Rated V_{DRM} or V_{RRM};		MAX	5		uA
Gate Trigger Current	I_{GT}	V_D=12V, R_L=33Ω	I-II-III	MAX	25	50	mA
			IV	MAX	50	100	
Gate Trigger Voltage	V_{GT}	V_D=12V, R_L = 33 kΩ		MAX	1.3		V
Gate Non−Trigger Voltage	V_{GD}	V_D = V_{DRM}, R_L = 33 kΩ, T_j = 125 °C		MIN	0.2		V
Peak Forward On-State Voltage	V_{TM}	IT=22.5A,		MAX	1.55		V
Latch Current	I_L	I_G = 1.2 I_{GT}	I-III-IV	MAX	40	60	mA
			II	MAX	80	120	
Holding Current	I_H	I_T=0.5A		MAX	25	50	mA
Critical Rate of Rise of Off-State Voltage	dV/dt	V_D=67%V_{DRM}, T_J=25°C, Gate open		MIN	200	400	V/μs

ELECTRICAL CHARACTERISTICS (TJ=25°C)
(3Q) Triggering in three quadran

Parameter	Symbol	Test Conditions			SW	CW	BW	Units
Peak Repetitive Forward or Reverse Blocking Current	I_{DRM} I_{RRM}	V_{AK} = Rated V_{DRM} or V_{RRM};		MAX	5			uA
Gate Trigger Current	I_{GT}	V_D=12V, R_L=33Ω	I-II-III	MAX	10	35	50	mA
Gate Trigger Voltage	V_{GT}	V_D=12V, R_L = 33 kΩ		MAX	1.3			V
Gate Non−Trigger Voltage	V_{GD}	V_D = V_{DRM}, R_L = 33 kΩ, T_j = 125 °C		MIN	0.2			V
Peak Forward On-State Voltage	V_{TM}	IT=22.5A,		MAX	1.55			V
Latch Current	I_L	I_G = 1.2 I_{GT}	I-III	MAX	25	50	70	mA
			II	MAX	30	60	80	
Holding Current	I_H	I_T=0.5A		MAX	15	35	50	mA
Critical Rate of Rise of Off-State Voltage	dV/dt	V_D=67%V_{DRM}, T_J=25°C, Gate open		MIN	40	400	1000	V/μs