

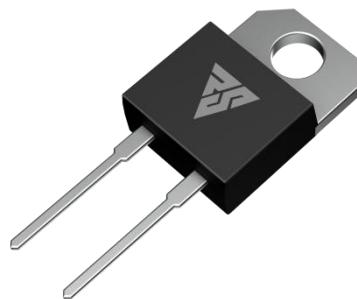
VRRM	IF ( TC=150°C)	QC
650V	8A	22nC

**Applications:**

- Power Factor Correction
- Sever Mode Power Supplies
- Uninterruptible Power Supply

**Features:**

- Low Forward Voltage Drop
- High-Speed Switching
- Positive Temperature Coefficient
- Temperature-Independent Switching Behavior


**Ordering Information**

Part Number	Package	Marking	Packing	Qty.
RSS08065B	TO-220-2	RSS08065B	Tube	50 PCS

**Maximum Ratings (TJ= 25°C unless otherwise specified)**

Symbol	Parameter	Value	Unit	Test Conditions	Note
VRRM	Repetitive Peak Reverse Voltage	650	V		
VRSM	Surge Peak Reverse Voltage	650	V		
VR	DC Blocking Voltage	650	V		
IF	Forward Current	8	A	TC = 150°C	Fig.7
IFSM	Non-Repetitive Forward Surge Current	75	A	TC = 25°C, tp = 10ms Half Sine Wave	
IF,Max	Non-Repetitive Peak Forward Surge Current	680	A	TC=25°C, tP= 10 μs, Pulse	
IFRM	Repetitive Peak Forward Surge Current	60	A	TC = 25°C, tp = 10ms Half Sine Wave	
Ptot	Power Dissipation	117 51	W	TC = 25°C TC = 110°C	Fig.6
TJ,TST G	Operating Junction and Storage Temperature	-55 to175	°C		

**Electrical Characteristics (TJ= 25°C unless otherwise specified)**

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
VF	Forward Voltage	1.4 1.7	1.7 2.0	V	IF =8A, TJ = 25°C IF =8A, TJ = 175°C	Fig.1
IR	Reverse Current	1 20	20 100	μA	VR =650V, TJ = 25°C VR = 650V, TJ = 175°C	Fig.2
C	Total Capacitance	400 44 38	/	pF	VR=0V, TJ = 25°C, f=1MHz VR=200V, TJ = 25°C, f=1MHz VR=400V, TJ = 25°C, f = 1MHz	Fig.3
QC	Total Capacitive Charge	22	/	nC	VR =400V, TJ = 25°C $Q_c = \int_0^{V_R} C(V) dV$	Fig.4
Ec	Capacitance Stored Energy	5.8	/	μJ	VR =400V	Fig.5

**Thermal Characteristics (TJ= 25°C unless otherwise specified)**

Symbol	Parameter	Typ.	Unit	Note
R <sub>θJC</sub>	Thermal Resistance from Junction to Case	2.3	°C/W	

### Typical Feature Curve

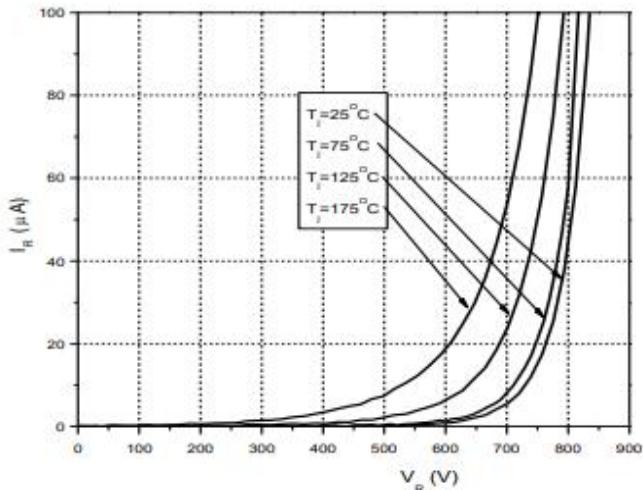
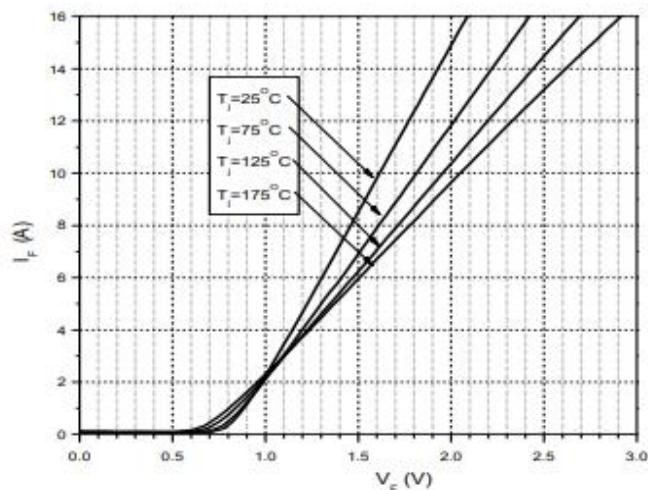


Figure 1. Forward Characteristics Figure 2. Reverse Characteristics

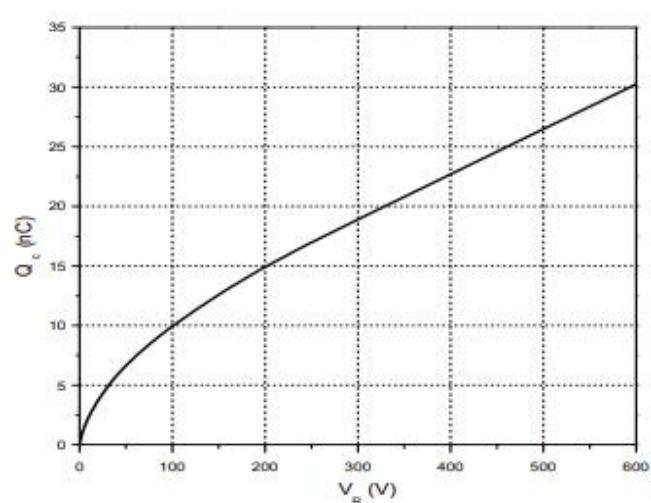
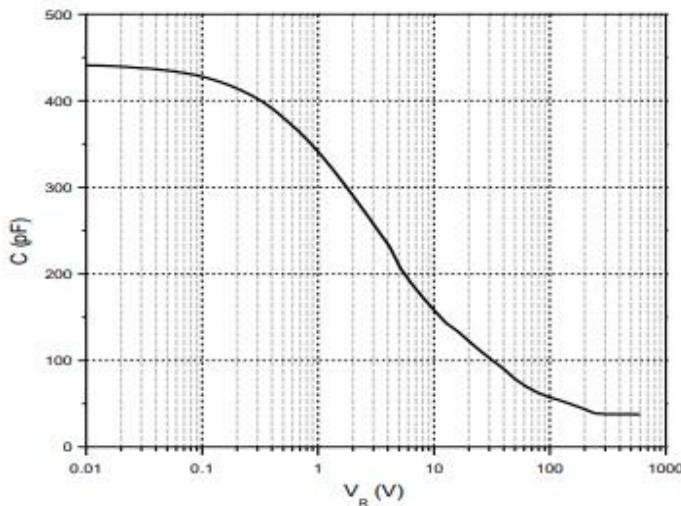


Figure 3. Capacitance vs. Reverse Voltage Figure 4. Total Capacitance Charge vs. Reverse Voltage

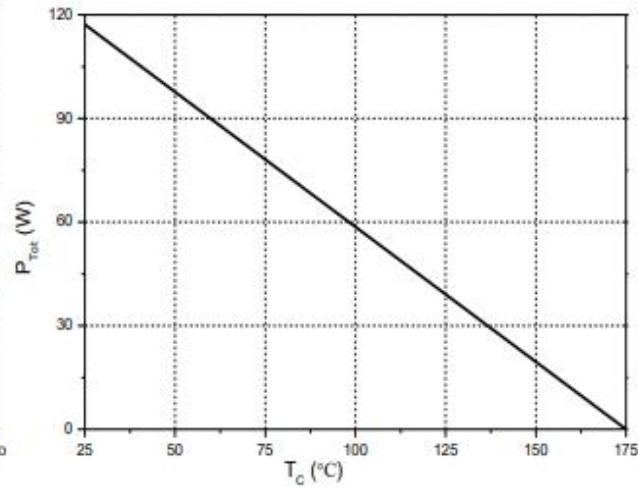
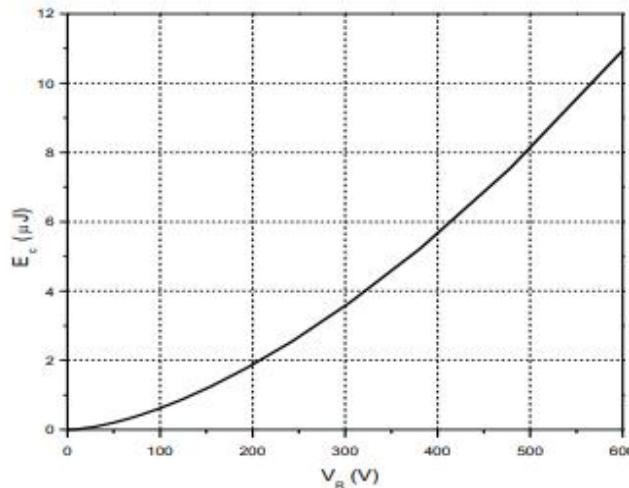


Figure 5. Capacitance Stored Energy Figure 6. Power Derating

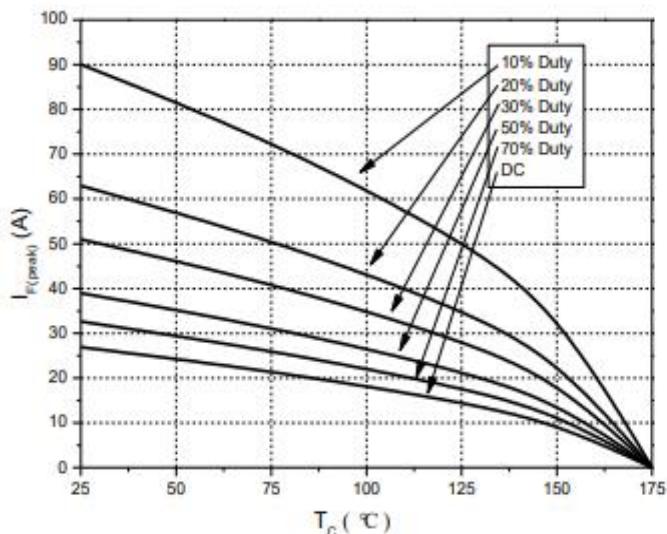


Figure 7. Current Derating

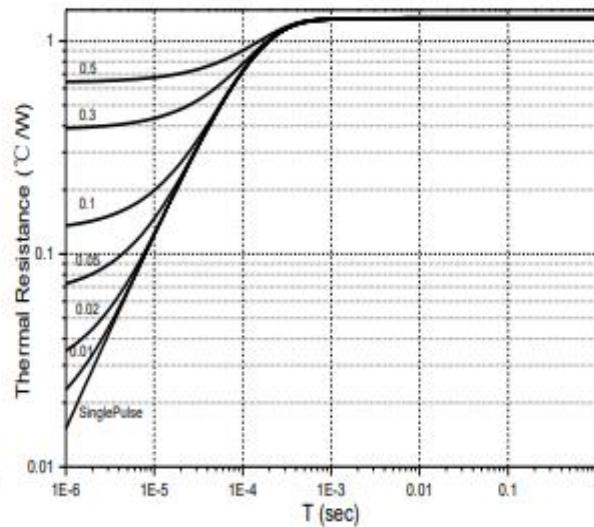
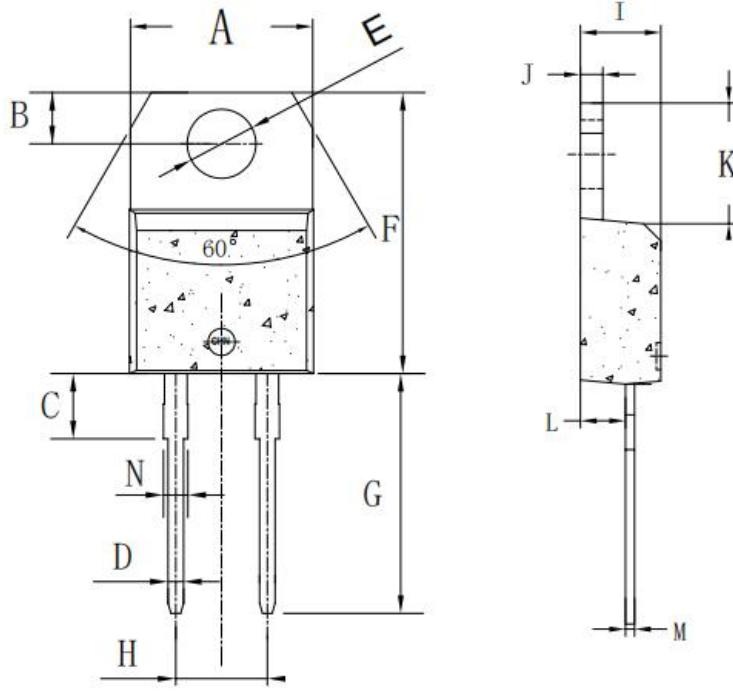


Figure 8. Transient Thermal Impedance

**Package outline drawing(TO-220 Unit: mm )**
**PACKAGE OUTLINE  
DIMENSIONS**  
**TO-220A-2L**


DIM.	Unit(mm)		Unit(inch)	
	Min	Max	Min	Max
<b>A</b>	9.8	10.4	0.385	0.409
<b>B</b>	2.65	3.1	0.104	0.122
<b>C</b>	2.8	4.2	0.110	0.165
<b>D</b>	0.7	0.92	0.027	0.036
<b>E</b>	3.75	3.95	0.147	0.155
<b>F</b>	14.8	16.1	0.582	0.633
<b>G</b>	13.05	13.6	0.513	0.535
<b>H</b>	4.9	5.3	0.192	0.208
<b>I</b>	4.38	4.61	0.172	0.181
<b>J</b>	1.15	1.36	0.045	0.053
<b>K</b>	5.85	6.82	0.230	0.268
<b>L</b>	2.35	2.75	0.092	0.108
<b>M</b>	0.35	0.65	0.013	0.025
<b>N</b>	1.18	1.42	0.046	0.055

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