



# BRT30N70P3

## N-channel Enhancement Mode Power MOSFET

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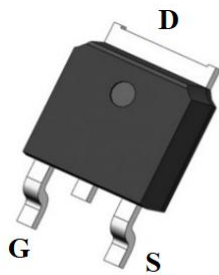
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## FEATURES

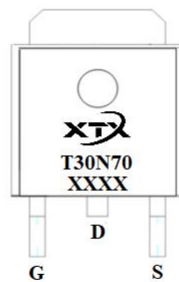
- ◆ 30V, 70A
- ◆  $R_{DS(ON)} < 6.0m\Omega @ V_{GS} = 10V$
- ◆  $R_{DS(ON)} < 9.5m\Omega @ V_{GS} = 4.5V$
- ◆ Advanced Trench Technology
- ◆ Excellent  $R_{DS(ON)}$  and Low Gate Charge
- ◆ Lead Free

## APPLICATIONS

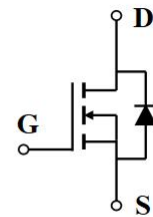
- ◆ Load Switch
- ◆ PWM Application
- ◆ Power Management



TO-252-2L Top View



Marking and Pin Assignment



Schematic Diagram

## PACKAGE MARKING AND ORDERING INFORMATION

OPN	Marking	Package	Quantity
BRT30N70P3	T30N70	TO-252-2L	2500pcs/Reel

## ABSOLUTE MAXIMUM RATINGS

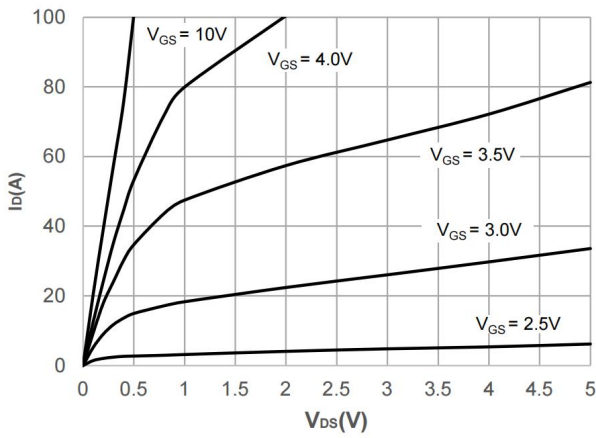
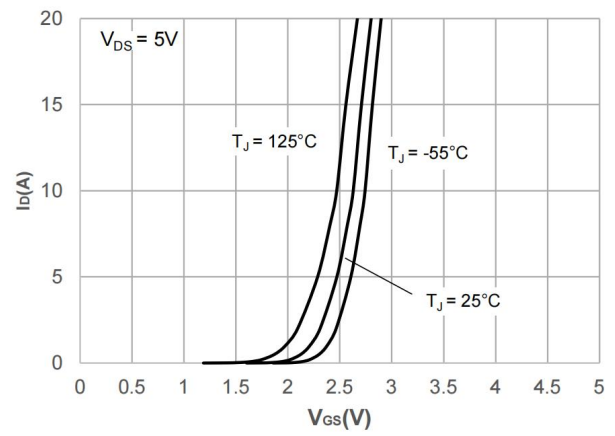
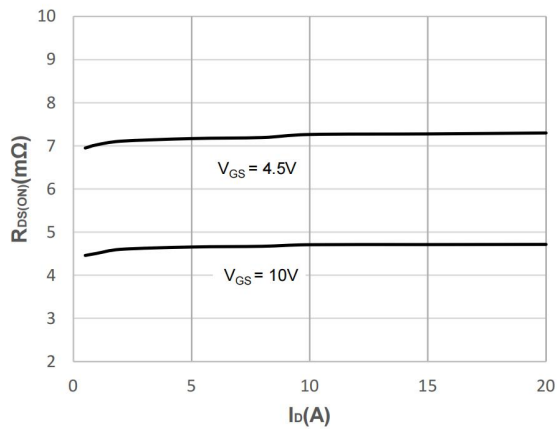
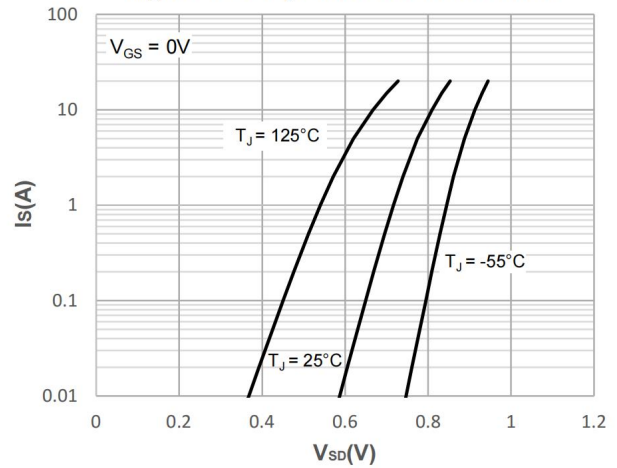
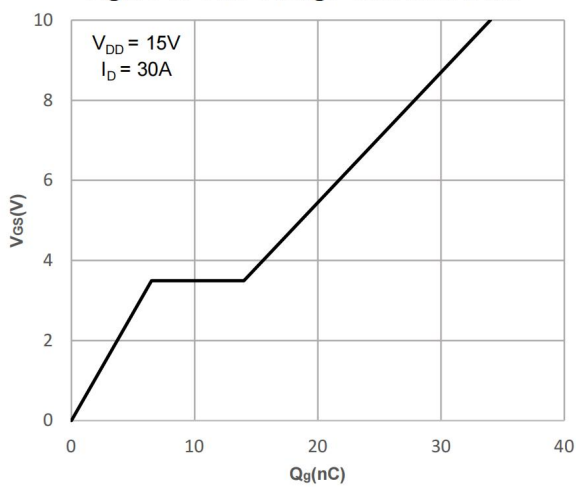
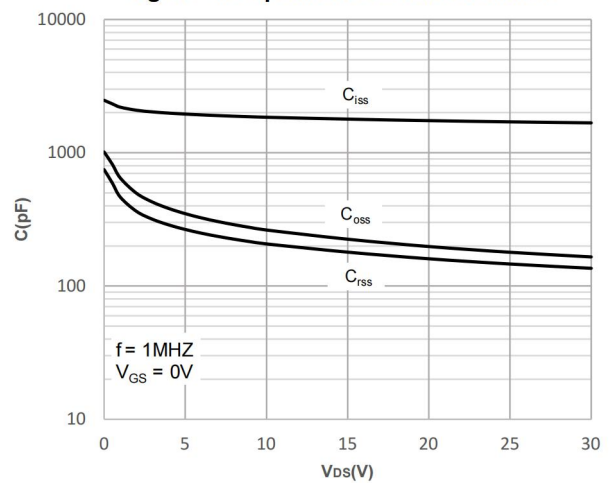
Symbol	Definition	Ratings	Unit	
$V_{DS}$	Drain-to-Source Voltage	30	V	
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V	
$I_D$	Continuous Drain Current	$T_C = 25^\circ C$	70	A
		$T_C = 100^\circ C$	45	A
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	280	A	
$E_{AS}$	Single Pulsed Avalanche Energy <sup>(2)</sup>	81	mJ	
$P_D$	Power Dissipation, $T_C = 25^\circ C$	50	W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>(3)</sup>	31	$^\circ C/W$	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.5	$^\circ C/W$	
$T_J, T_{STG}$	Junction & Storage Temperature Range	-55 ~ +150	$^\circ C$	

**ELECTRICAL CHARACTERISTICS** (All test condition is  $T_J=25^{\circ}\text{C}$ , unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	1.6	2.5	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance <sup>(4)</sup>	$V_{GS} = 10\text{V}, I_D = 30\text{A}$		4.0	6.0	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$		6.1	9.5	$\text{m}\Omega$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 15\text{V},$ $f = 1\text{MHz}$	-	1899	-	pF
$C_{oss}$	Output Capacitance		-	221	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	191	-	pF
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 15\text{V}, I_D = 30\text{A}$	-	34	-	nC
$Q_{gs}$	Gate Source Charge		-	6.5	-	nC
$Q_{gd}$	Gate Drain("Miller") Charge		-	7.5	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DD} = 15\text{V}$ $I_D = 30\text{A}, R_{GEN} = 3\Omega$	-	7	-	ns
$t_r$	Turn-On Rise Time		-	14	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	34	-	ns
$t_f$	Turn-Off Fall Time		-	11	-	ns
<b>Drain-Source Diode Characteristics</b>						
$I_S$	Continuous Source Current		-	-	70	A
$V_{SD}$	Forward on voltage	$V_{GS} = 0\text{V}, I_S = 30\text{A}$	-	-	1.2	V
$T_{rr}$	Reverse Recovery Time	$I_F = 20\text{A}, di/dt = 100\text{A}/\mu\text{s}$	-	10	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	1.7	-	nC

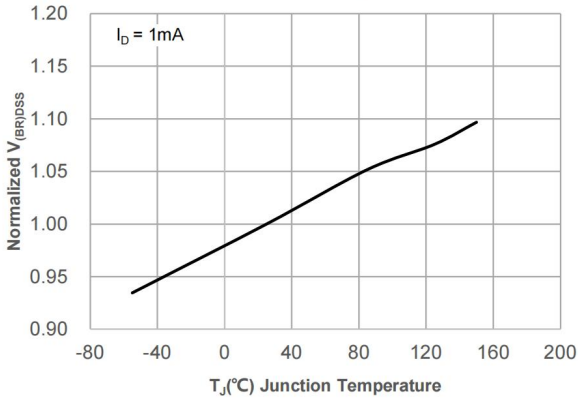
Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2.  $E_{AS}$  condition: Starting  $T_J=25^{\circ}\text{C}$ ,  $V_{DD}=15\text{V}$ ,  $V_G=10\text{V}$ ,  $R_G=25\Omega$ ,  $L=0.5\text{mH}$ ,  $I_{AS}=18\text{A}$
3.  $R_{\theta JA}$  is measured with the device mounted on a 1 inch<sup>2</sup> pad of 2oz copper FR4 PCB
4. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$ .

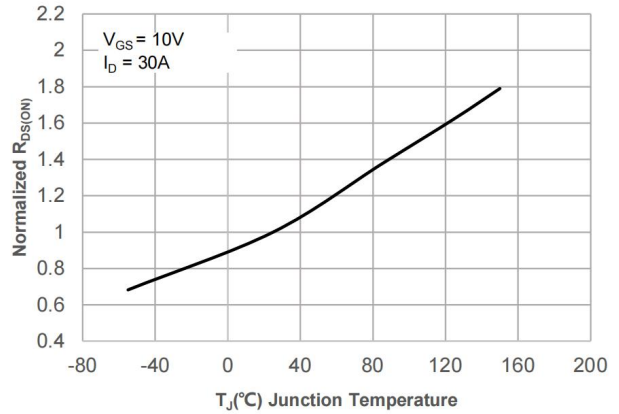
**TYPICAL PERFORMANCE CHARACTERISTICS**
**Figure 1: Output Characteristics**

**Figure 2: Typical Transfer Characteristics**

**Figure 3: On-resistance vs. Drain Current**

**Figure 4: Body Diode Characteristics**

**Figure 5: Gate Charge Characteristics**

**Figure 6: Capacitance Characteristics**


**TYPICAL PERFORMANCE CHARACTERISTICS**

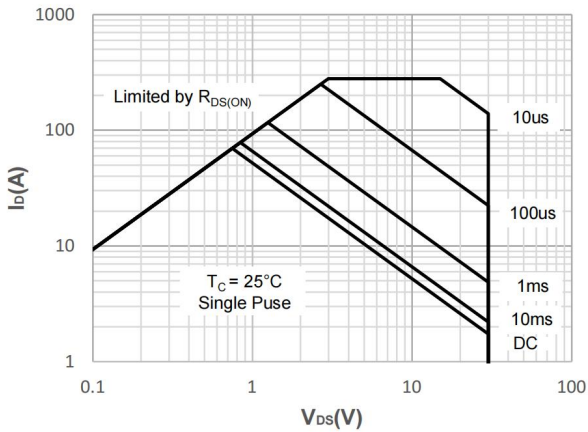
**Figure 7: Normalized Breakdown voltage vs. Junction Temperature**



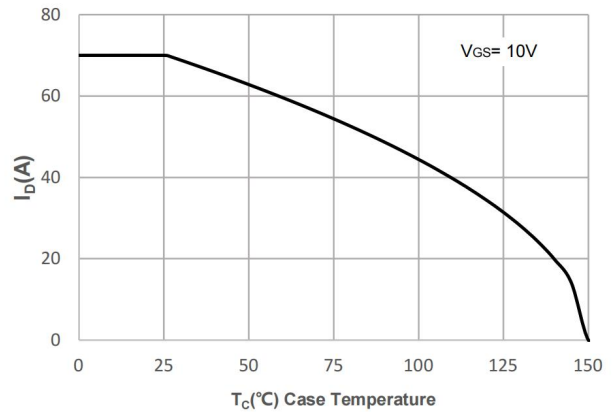
**Figure 8: Normalized on Resistance vs. Junction Temperature**



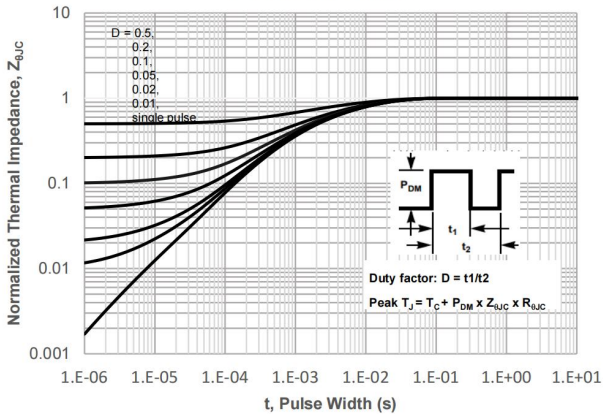
**Figure 9: Maximum Safe Operating Area**



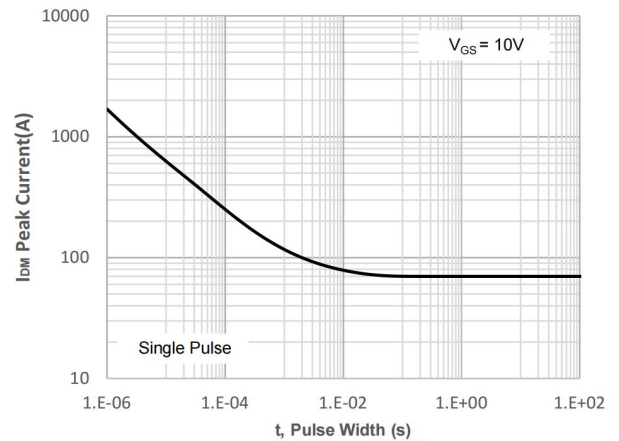
**Figure 10: Maximum Continuous Drain Current vs. Case Temperature**



**Figure 11: Normalized Maximum Transient Thermal Impedance**



**Figure 12: Peak Current Capacity**



TEST CIRCUIT

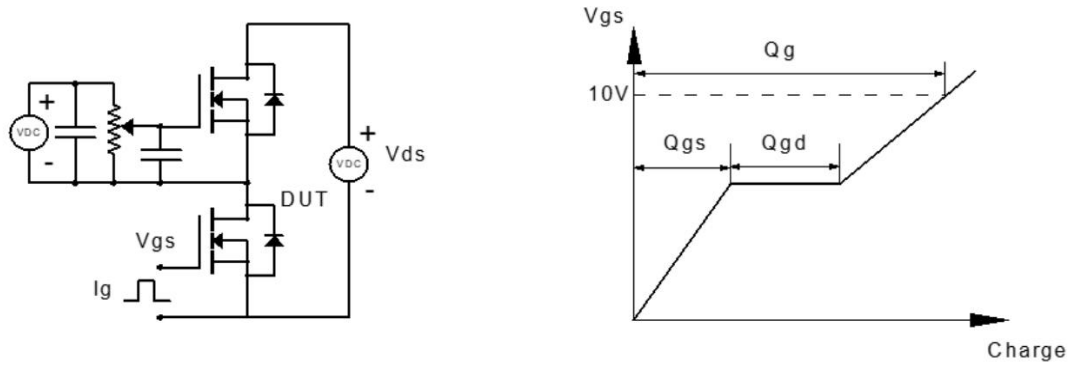


Figure 13: Gate Charge Test Circuit & Waveform

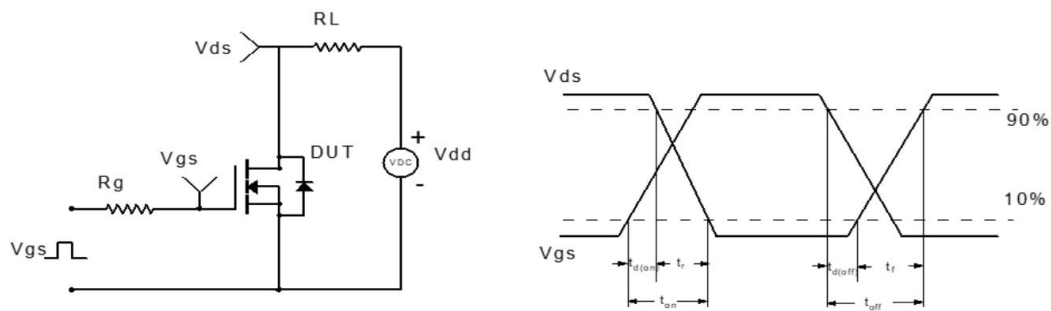


Figure 14: Resistive Switching Test Circuit & Waveform

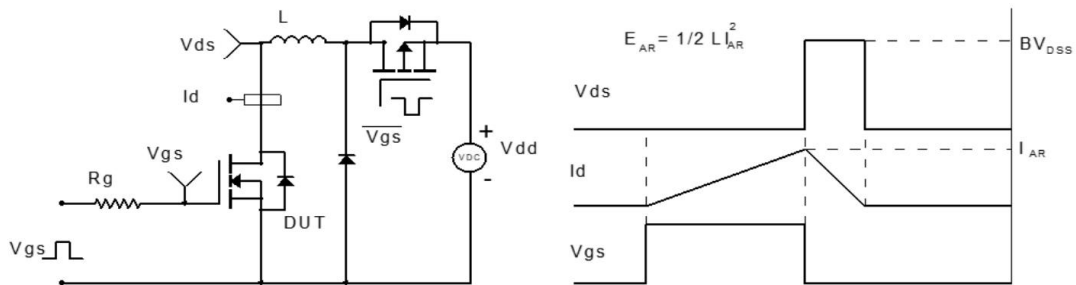


Figure 15: Unclamped Inductive Switching Test Circuit & Waveform

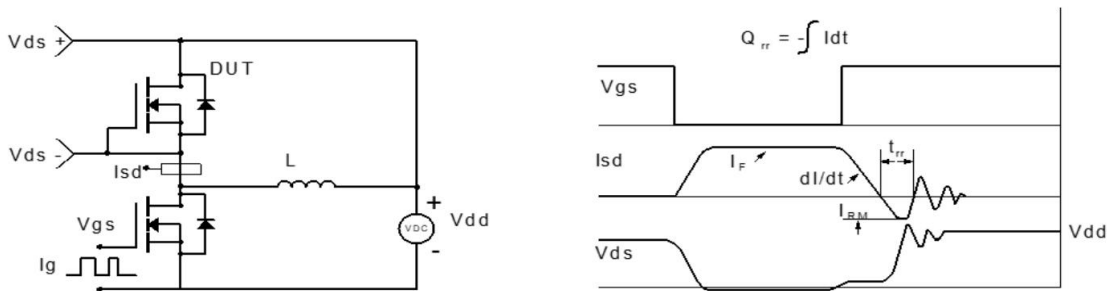
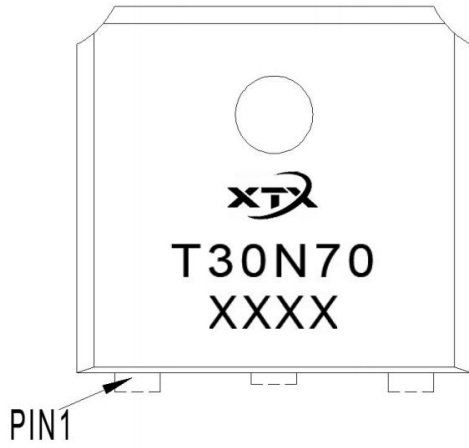


Figure 16: Diode Recovery Test Circuit & Waveform

**MARKING INFORMATION**



1st Line: XTX Logo

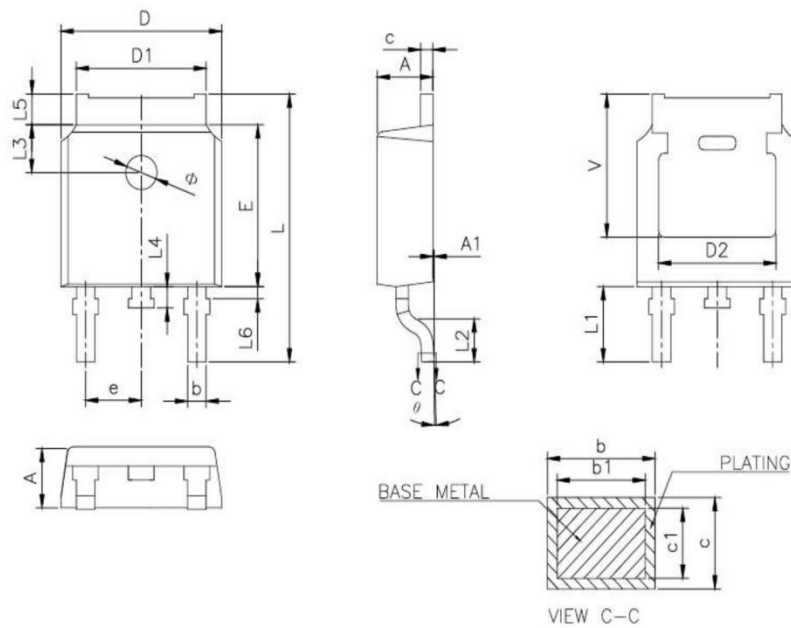
2nd Line: Part Number ( T30N70 )

3rd Line: Date Code ( XXXX )

XX: Year

XX: Week ( 01 to 53 )

Year	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Code	21	22	23	24	25	26	27	28	29	30	31	32	33

**DETAIL PACKAGE OUTLINE DRAWING (TO-252-2L)**


SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	-	0.10
b	0.66	-	0.86
b1	0.65	0.76	0.81
c	0.47	-	0.60
c1	0.46	0.51	0.56
D	6.50	6.60	6.70
D1	5.10	5.33	5.46
D2	4.83 REF.		
E	6.00	6.10	6.20
e	2.186	2.286	2.386
L	9.80	10.10	10.40
L1	2.90 REF.		
L2	1.40	1.50	1.60
L3	1.80 REF.		
L4	0.60	0.80	1.00
L5	0.90	-	1.25
L6	0.15	-	0.75
Φ	1.10	-	1.30
θ	0		8°
V	5.40 REF.		



**REVISION HISTORY**

<b>Number</b>	<b>Description</b>
Rev 1.0	BRT30N70P3 datasheet release