



BRT40N60P3

N-channel Enhancement Mode Power MOSFET

芯天下技术股份有限公司

XTX Technology Inc.

Tel: (+86 755) 28229862

Fax: (+86 755) 28229847

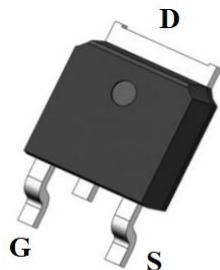
Web Site: <http://www.xtxtech.com/>

Technical Contact: fae@xtxtech.com

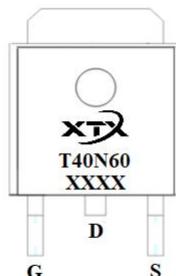
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FEATURES

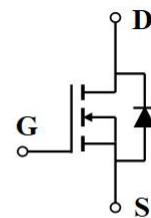
- ◆ 40V, 60A
- $R_{DS(ON)} < 7.0\text{m}\Omega$ @ VGS = 10V
- $R_{DS(ON)} < 12\text{m}\Omega$ @ VGS = 4.5V
- ◆ Advanced Trench Technology
- ◆ Excellent $R_{DS(ON)}$ and Low Gate Charge
- ◆ Lead Free



TO-252-2L Top View



Marking and Pin Assignment



Schematic Diagram

PACKAGE MARKING AND ORDERING INFORMATION

OPN	Marking	Package	Quantity
BRT40N60P3	T40N60	TO-252-2L	2500pcs/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition		Ratings	Unit
V_{DS}	Drain-to-Source Voltage		40	V
V_{GS}	Gate-to-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	60	A
		$T_C = 100^\circ\text{C}$	38	A
I_{DM}	Pulsed Drain Current ⁽¹⁾		240	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾		100	mJ
P_D	Power Dissipation, $T_C = 25^\circ\text{C}$		114	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾		40	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.5	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Junction & Storage Temperature Range		-55 ~ +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (All test condition is $T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{TH})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1.1	1.6	2.5	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}$, $I_D = 30\text{A}$		5.6	7	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}$, $I_D = 20\text{A}$		7.0	12	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 20\text{V}$, $f = 1\text{MHz}$	-	2396	-	pF
C_{oss}	Output Capacitance		-	162	-	pF
C_{rss}	Reverse Transfer Capacitance		-	138	-	pF
R_G	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1.0\text{MHz}$	-	1.97	-	Ω
Q_g	Total Gate Charge	$V_{GS} = 0$ to 10V $V_{DS} = 20\text{V}$, $I_D = 20\text{A}$	-	48	-	nC
Q_{gs}	Gate Source Charge		-	10	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	10	-	nC
Switching Characteristics						
$t_{d(\text{on})}$	Turn-On Delay Time	$V_{GS} = 10\text{V}$, $V_{DD} = 20\text{V}$ $I_D = 20\text{A}$, $R_G = 3\Omega$	-	10	-	ns
t_r	Turn-On Rise Time		-	28	-	ns
$t_{d(\text{off})}$	Turn-Off Delay Time		-	38	-	ns
t_f	Turn-Off Fall Time		-	9	-	ns
Drain-Source Diode Characteristics						
I_S	Continuous Source Current		-	-	60	A
V_{SD}	Forward on voltage	$V_{GS} = 0\text{V}$, $I_S = 30\text{A}$	-	-	1.2	V
T_{rr}	Reverse Recovery Time	$I_F = 20\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$	-	11	-	ns
Q_{rr}	Reverse Recovery Charge		-	5	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=20\text{V}$, $V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=20\text{A}$
3. R_{0JA} is measured with the device mounted on a 1 inch² pad of 2oz copper FR4 PCB
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 1: Output Characteristics

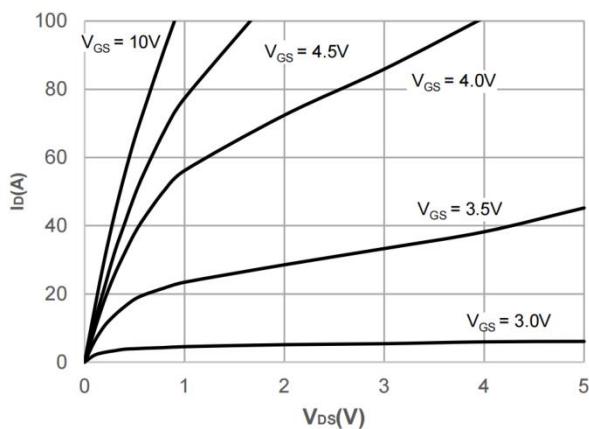


Figure 2: Typical Transfer Characteristics

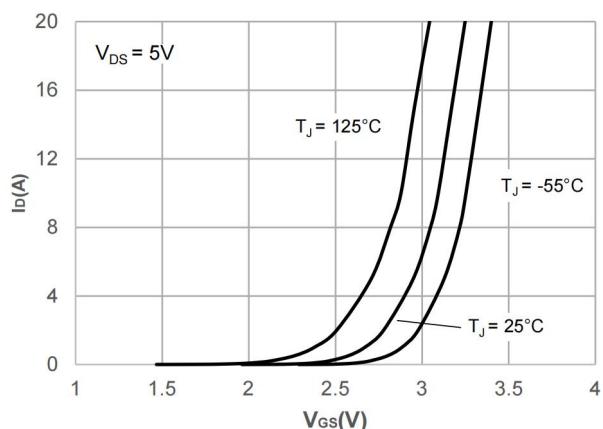


Figure 3: On-resistance vs. Drain Current

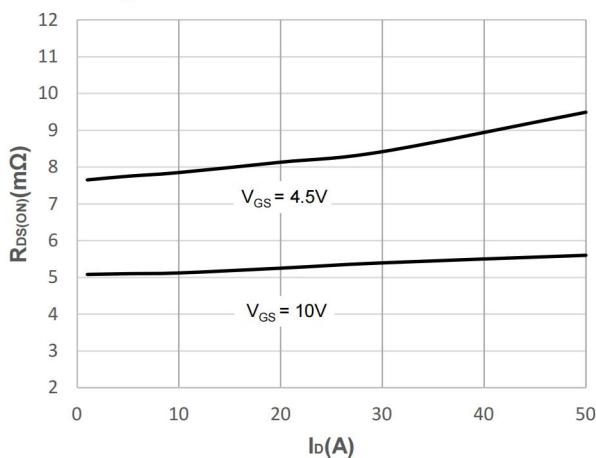


Figure 4: Body Diode Characteristics

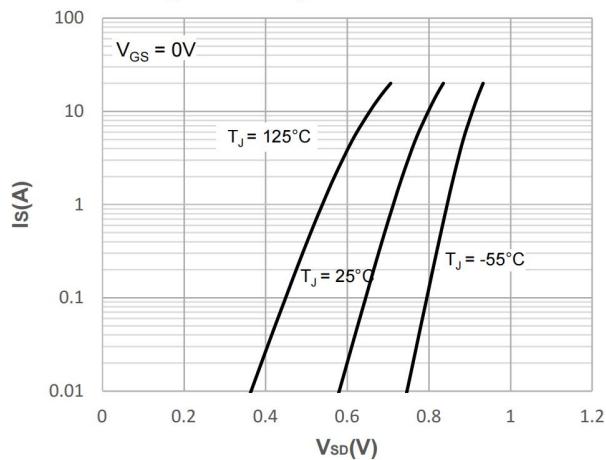


Figure 5: Gate Charge Characteristics

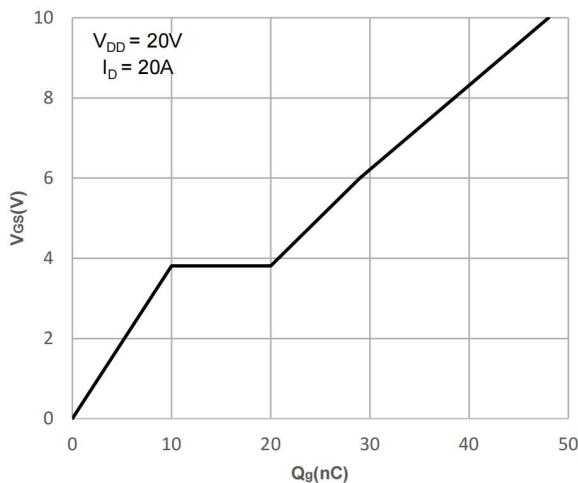
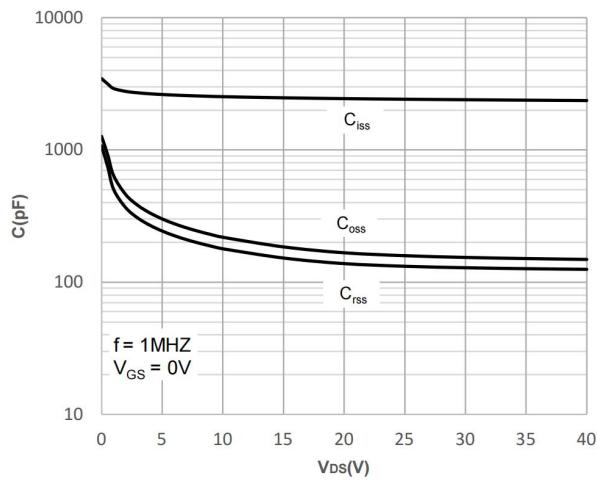


Figure 6: Capacitance Characteristics



TYPICAL PERFORMANCE CHARACTERISTICS

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

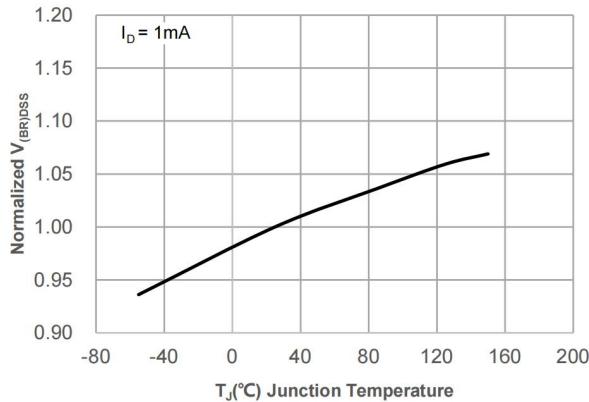


Figure 8: Normalized on Resistance vs. Junction Temperature

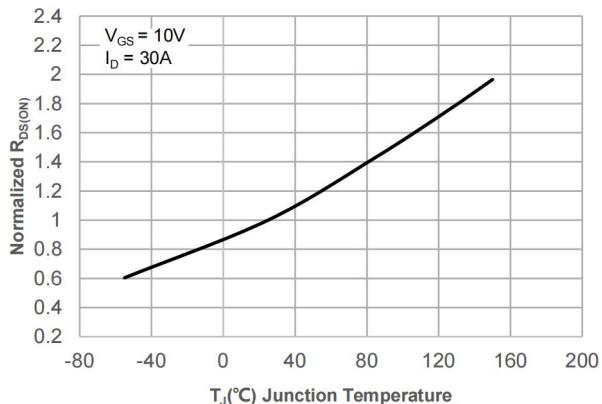


Figure 9: Maximum Safe Operating Area

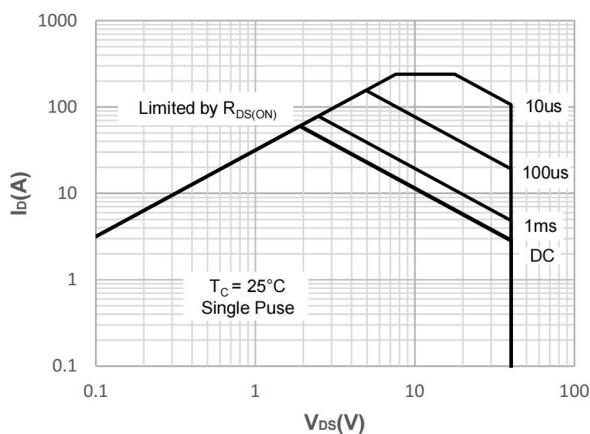


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

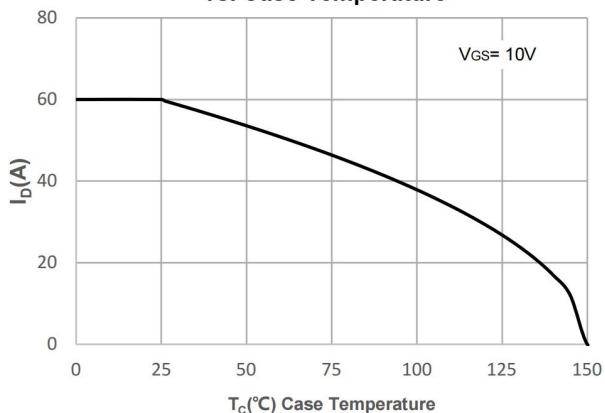


Figure 11: Normalized Maximum Transient Thermal Impedance

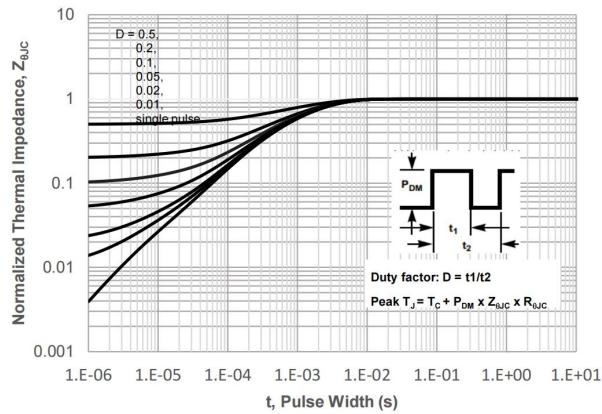
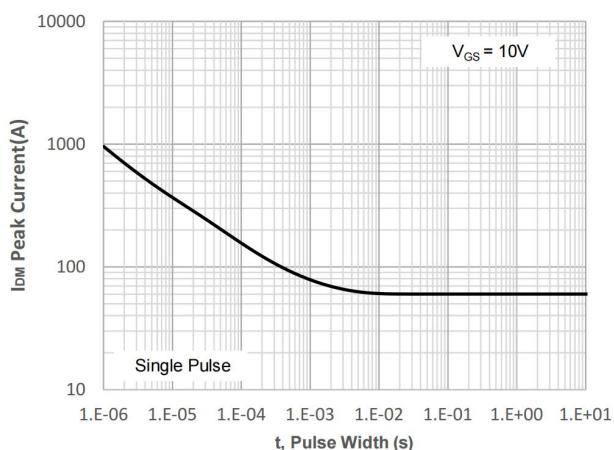


Figure 12: Peak Current Capacity



TEST CIRCUIT

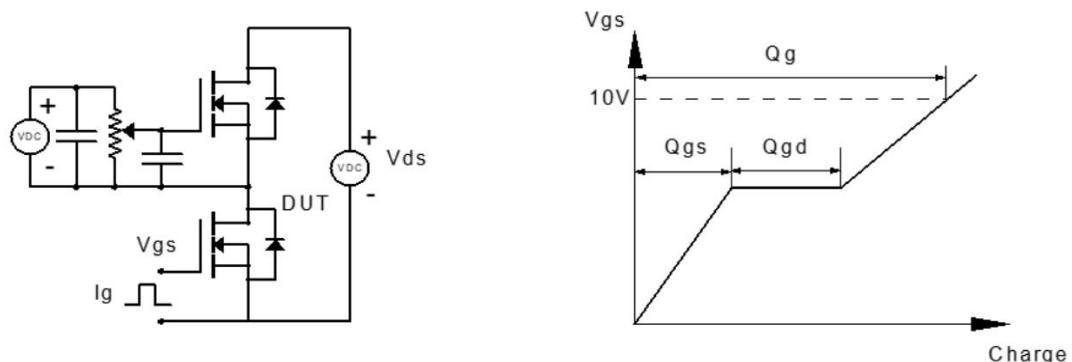


Figure 13: Gate Charge Test Circuit & Waveform

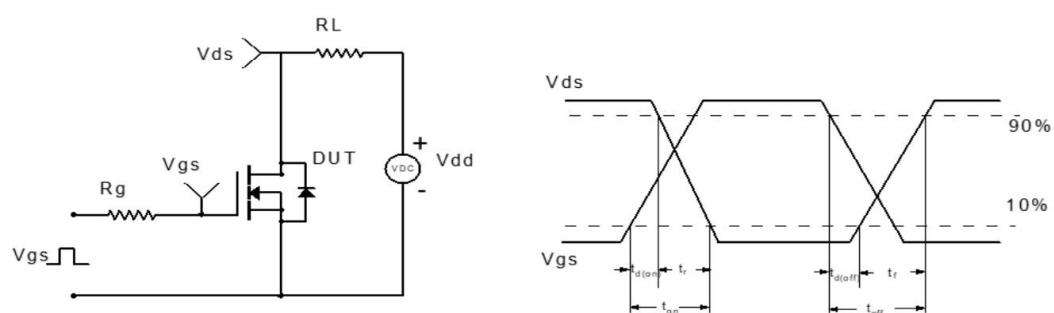


Figure 14: Resistive Switching Test Circuit & Waveform

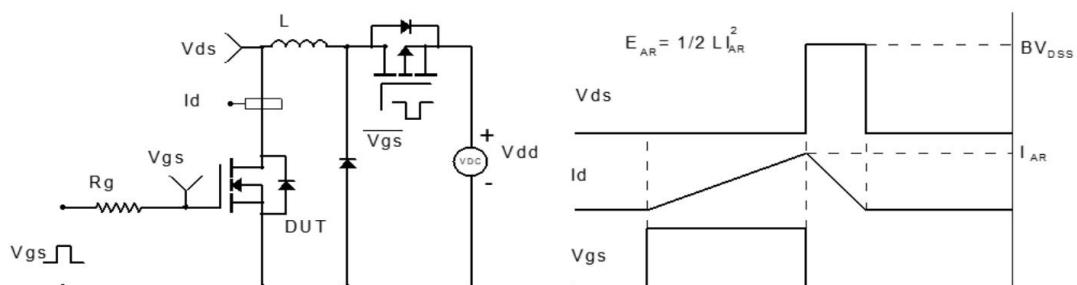


Figure 15: Unclamped Inductive Switching Test Circuit & Waveform

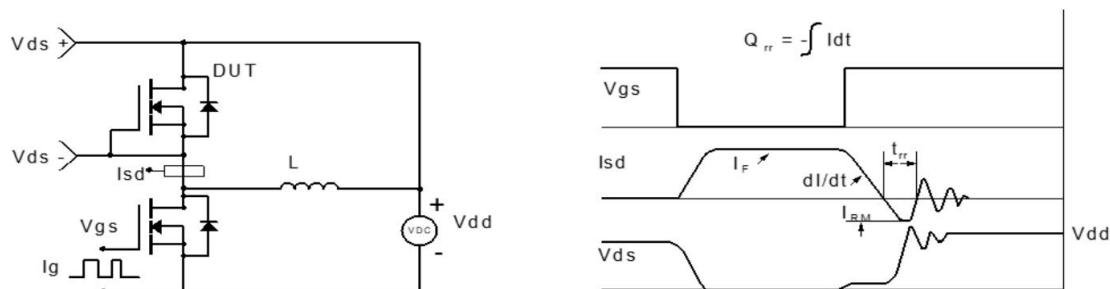
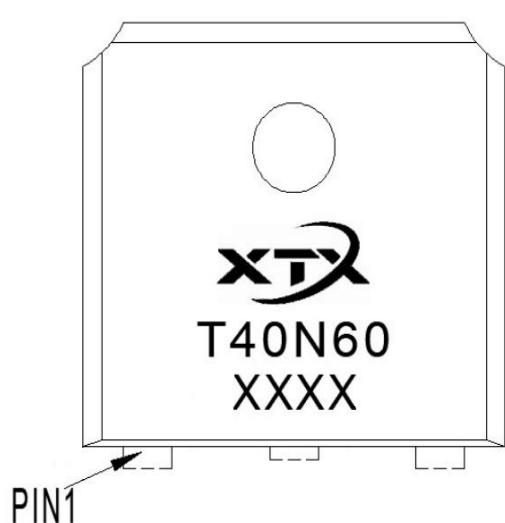


Figure 16: Diode Recovery Test Circuit & Waveform

MARKING INFORMATION

1st Line: XTX Logo

2nd Line: Part Number (T40N60)

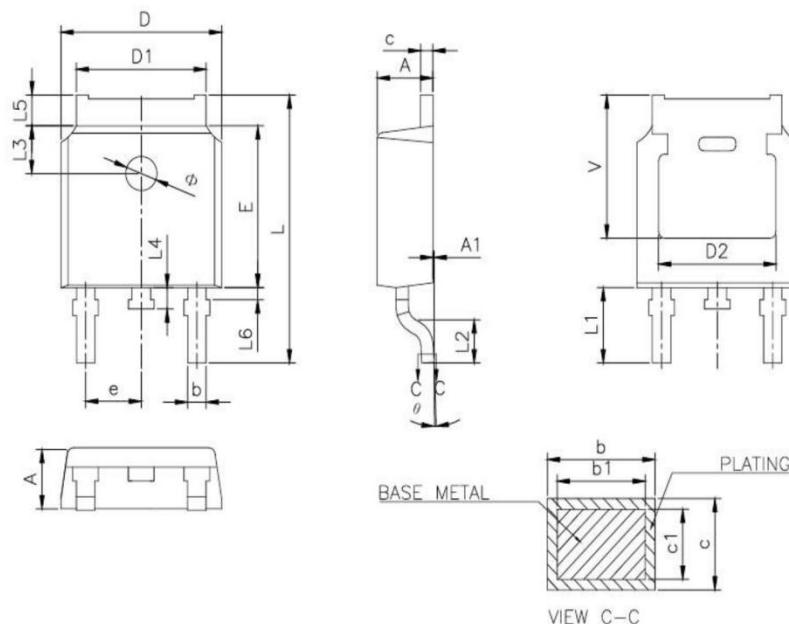
3rd Line: Date Code (XXXX)

XX: Year

XX: Week (01 to 53)

Year	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Code	21	22	23	24	25	26	27	28	29	30	31	32	33

DETAIL PACKAGE OUTLINE DRAWING (TO-252-2L)



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	-	0.10
b	0.66	-	0.86
b1	0.65	0.76	0.81
c	0.47	-	0.60
c1	0.46	0.51	0.56
D	6.50	6.60	6.70
D1	5.10	5.33	5.46
D2	4.83 REF.		
E	6.00	6.10	6.20
e	2.186	2.286	2.386
L	9.80	10.10	10.40
L1	2.90 REF.		
L2	1.40	1.50	1.60
L3	1.80 REF.		
L4	0.60	0.80	1.00
L5	0.90	-	1.25
L6	0.15	-	0.75
Φ	1.10	-	1.30
θ	0		
V	5.40 REF.		

REVISION HISTORY

Number	Description
Rev 1.0	BRT40N60P3 datasheet release